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# Test system of the front-end readout for an application-specific integrated circuit for the water Cherenkov detector array at the large high-altitude air shower observatory

Er-Lei Chen[1,2] · Lei Zhao[1,2] · Li Yu[1,2] · Jia-Jun Qin[1,2] · Yu Liang[1,2] · Shu-Bin Liu[1,2] · Qi An[1,2]

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**Abstract** The water Cherenkov detector array (WCDA) is an important part of the large high-altitude air shower observatory (LHAASO), which is in a research and development phase. The central scientific goal of LHAASO is to explore the origin of high-energy cosmic rays of the universe and to push forward the frontier of new physics. To simplify the WCDA's readout electronics, a prototype of a front-end readout for an application-specific integrated circuit (ASIC) is designed based on the time-over-threshold method to achieve charge-to-time conversion. High-precision time measurement and charge measurement are necessary over a full dynamic range [1–4000 photoelectrons (P.E.)]. To evaluate the performance of this ASIC, a test system is designed that includes the front-end ASIC test module, digitization module, and test software. The first module needs to be customized for different ASIC versions, whereas the digitization module and test software are tested for general-purpose use. In the digitization module, a field programmable gate array-based time-to-digital converter is designed with a bin size of 333 ps, which also integrates an inter-integrated circuit to configure the ASIC test module, and a universal serial bus interface is designed to transfer data to the remote computer. Test results indicate that the time resolution is better than 0.5 ns, and the charge resolution is better than 30% root mean square (RMS) at 1 P.E. and 3% RMS at 4000 P.E., which are beyond the application requirements.

**Keywords** Time and charge measurement · Photomultiplier tube (PMT) · Water Cherenkov detector array · Inter-integrated circuit · Application-specific integrated circuit · Test system

## 1 Introduction

### 1.1 Background and physical objective

The large high-altitude air shower observatory (LHAASO) is oriented to study and observe the high-energy cosmic rays of the universe. It consists of several detector systems: a 1-km$^2$ complex array; a wide FOV Cherenkov telescope array; a 100-m$^2$ high threshold core detector array; and a 90,000-m$^2$ water Cherenkov detector array (WCDA) [1]. The WCDA is one of the major components of the LHAASO project [2, 3], which consists of four 150 m × 150 m water ponds. As shown in Fig. 1, each pond is divided into 30 × 30 cells, and each cell has one photomultiplier tube (PMT) facing upward toward the bottom center of the cell to collect the Cherenkov light produced by the shower particles in water [4].

Figure 2 illustrates an air shower detected by the PMTs in the WCDA. The kernel task of the WCDA has two jobs: (1) The time measurement of secondary particles is used to determine the incidence direction of the air shower and (2)

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✉ Lei Zhao
zlei@ustc.edu.cn

[1] State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China

[2] Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China

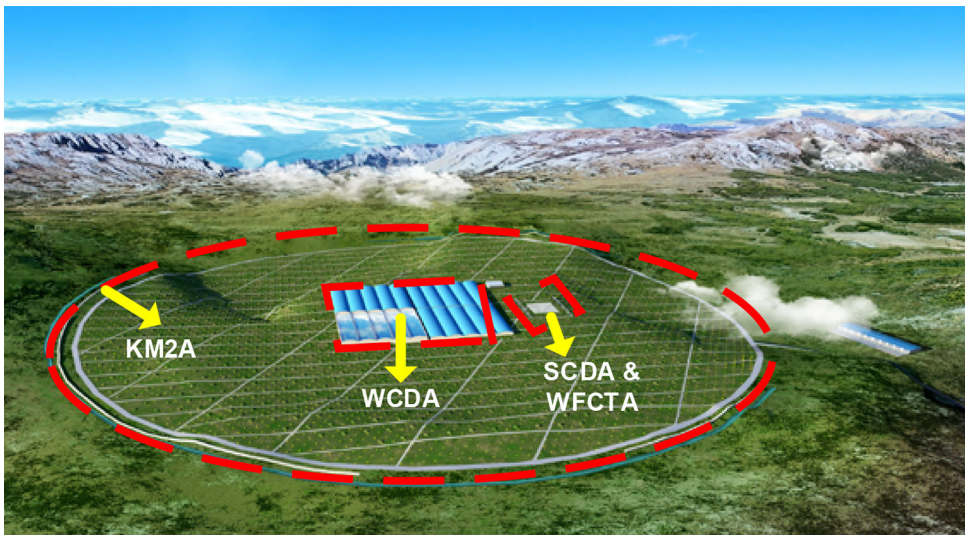


**Fig. 1** (Color online) WCDA in LHAASO project

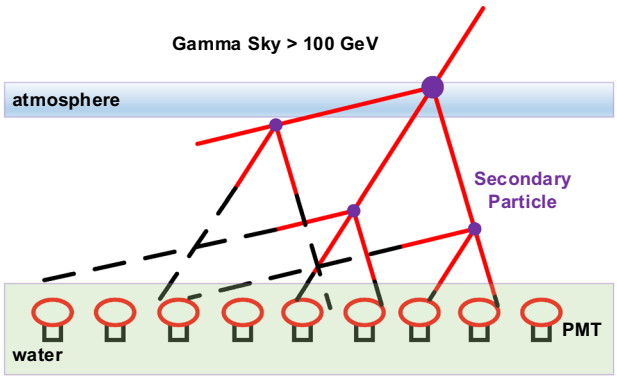


**Fig. 2** (Color online) Block diagram of the Gamma ray detected by the PMT

the charge measurement is used to obtain particle identification and energy information.

### 1.2 Requirements

According to the application requirements and performance of the detectors, Table 1 lists the WCDA readout electronics. To target the research purpose, the amount of the Cherenkov light (corresponding to the charge information of the PMT output signal) and its arrival time on the PMTs both need to be measured efficiently. The amplitude of the smallest signal, 1 photoelectron (P.E.), is as low as 60 μA, with a leading edge of 4 ns and a trailing edge of 16 ns. A large dynamic range from 1 to 4000 P.E. (0.75–3000 pC) is required. The charge measurement requirement is equivalent to an effective number of bits of around 13.3 bit of analog-to-digital converter.

To simplify the structure of the front-end electronics, a front-end readout for an application-specific integrated circuit (ASIC) is designed. The PMT signal is imported to the leading-edge discrimination circuit for time measurement and then is converted to a pulse width for charge-to-time conversion based on the time-over-threshold method. A test system is designed to evaluate the performance of this ASIC. The output of the ASIC is fed to a field programmable gate array (FPGA)-based time-to-digital converter (TDC) for digitization, and then, the resulting data are read through a universal serial bus (USB) interface.

### 1.3 State-of-the-art applications

We investigated this method using similar time digitization systems. Their performance is listed in Table 2.

Compared with ASIC-based TDC, the FPGA-based TDC reduces system complexity while also providing good flexibility [10], because the TDC and control logic, as well as the data-transferring interface, can be integrated within a single FPGA device. As for the FPGA-based TDCs, the

**Table 1** Measurement requirement of the WCDA readout electronics

| Items | Requirements |
|---|---|
| Channel number | 3600 |
| Bin size of time measurement | <1 ns |
| Root mean square (RMS) of time measurement | <500 ps |
| Dynamic range of charge measurement | S.P.E. ~4000 P.E. |
| Resolution of charge measurement (relative resolution) | 3% RMS at 4000 P.E., 30% RMS at S.P.E. |

**Table 2** Comparison of advantages and disadvantages of different TDC methods

| Methods | Bin Size (least significant bits) | Resource consumption | Dynamic range | Types | Flexibilities | Development period |
|---|---|---|---|---|---|---|
| Counter [5] | 25 ns | – | >1 s | FPGA | Good | Short |
| Delay cell [6] interpolation | 15 ps | – | – | FPGA | Good | Short |
| Multi-phase clock [7] interpolation | 625 ps | – | >1 s | FPGA | Good | Short |
| Wave Union [8] | 10 ps | 2081 Slice Register & 3280 LUT | <1 μs | FPGA | Good | Short |
| HPTDC [9] | 25 ps | – | 100 μs | ASIC | Poor | Long |

time resolution for a counter-based method is limited. With the interpolation method using special delay cells in the FPGAs, time resolution can be greatly improved. In particular, when using the wave union technique, a resolution of 10 ps was successfully achieved. Because special resources are needed, the high cost for logic consumption is problematic. This paper aims to design an FPGA-based TDC with a bin size of around 330 ps and low resource consumption (presented in Sect. 3.2).

## 2 Architecture of the test system

Figure 3 shows the structure of the WCDA readout electronics. To achieve a large dynamic range, signals are read out from the PMT's anode and dynode. The ASIC anode channel covers a range from 1 to 100 P.E., whereas the dynode channel covers a range from 40 to 4000 P.E. The signal is input to the ASIC's discriminator for time measurement and is converted to a pulse width through charge-to-time converters (QTC) based on the current-mode linear-discharging method. With the FPGA-based TDC, time and charge information can be digitized simultaneously. Measurement results are packaged based on the Transmission Control Protocol/Internet Protocol standard. These results then are sent through a GTX transceiver and an optical transceiver to the clock-and-data transfer module for data accumulation; finally, results are transferred to data acquisition for data analysis.

Figure 4 shows the block diagram of one channel of the ASIC prototype. In the ASIC, the anode and dynode signals are converted to a pulse width (Q_pulse in Figs. 4, 5), which corresponds to the input signal charge information. The anode signal also is fed to the discriminator in the ASIC for time measurement, and the output is marked as T_pulse in Figs. 4 and 5. In the current version, a total of two channels are integrated in a 3 mm × 3 mm block with 0.35-μm complementary metal oxide semiconductors technology. After confirming basic functionality and performance in the current version, additional channels will be integrated in subsequent ASIC versions.

Systematic tests must be conducted to evaluate whether the chip's performance can achieve the experiment's target. A test system is designed to accommodate different versions of the ASIC.

As shown in Fig. 5, the whole test system has three parts: the front-end module, digitization module, and test software. The ASIC being tested is placed on the front-end module with power supplies and input/output connectors. This module should be adapted for different ASIC

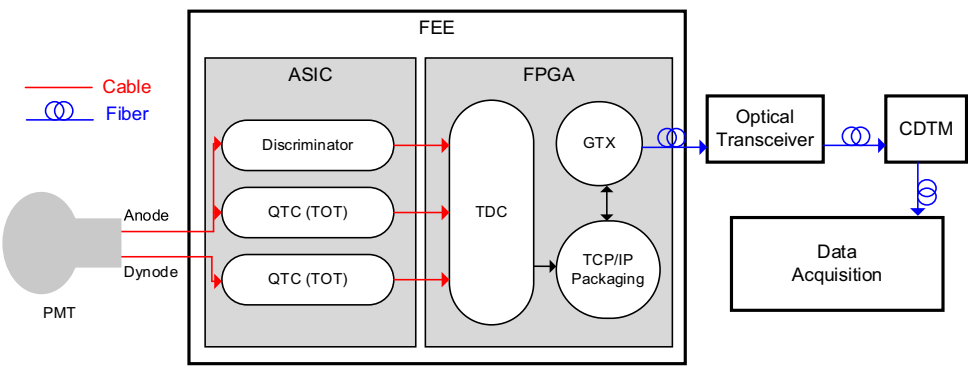


**Fig. 3** (Color online) Block diagram of the WCDA readout electronics (one channel)

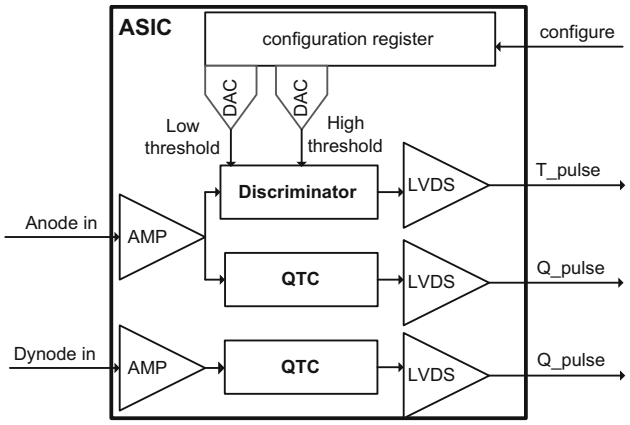


**Fig. 4** Block diagram of the ASIC (each channel) [11]

versions, and the digitization module should be designed for general-purpose use. The digitization module imports signals from the ASIC module, integrates the TDC in one FPGA for time digitization, and uses an inter-integrated circuit ($I^2C$) interface logic to configure the ASIC and USB interface for data readout. The test software is designed based on Visual C++ for data readout and hardware configuration. Considering the simple structure of the ASIC module, this paper focuses on the digitization module and the test software, which are presented in the following sections.

## 3 Structure of the test module

### 3.1 Serial interface logic design for ASIC configuration

The $I^2C$ protocol is used widely in ASIC configuration, considering the following advantages: The validity of data transfer is guaranteed by the acknowledgment process, different registers can be accessed by addresses, and all $I^2C$ devices are designed to communicate on the shared two-wire bus (i.e., featuring a simple structure).

We designed an $I^2C$ interface logic to configure the ASIC chip and other peripheral devices on the front-end module. The structure of the Algorithmic State Machine (ASM) is shown in Fig. 6. The logic was designed with Verilog Hardware Description Language on Quartus® II 13.1 and was implemented on an Intel® (Santa Clara, CA) FPGA EP3C55F780 (formerly Altera; San Jose, CA).

To confirm the logic functionality, we conducted simulations. Figure 7 shows the functional simulation results of the three wire signals, including the serial data (SDA, containing addresses and data), serial clock (SCL), and the write start (WR) signal, which agree with the expected results. As shown in Fig. 7, a HIGH to LOW transition on the SDA line, while SCL is HIGH, acts as a START signal, whereas a LOW to HIGH transition on the SDA line, while SCL is HIGH, acts as a STOP signal. The receiver is obliged to generate an acknowledgment ("Ack1, 2, 3, 4" in Fig. 7) after each byte is received. In Fig. 7, a total of four bytes are transferred successfully in the simulation. The first byte contains the address of the receiver, whereas the following three bytes include the user command and data information.

### 3.2 TDC integrated in the FPGA

To digitize the output signals from the ASIC, we designed a TDC based on an FPGA and time interpolation method [12]. The designed logic about TDC is implemented in an Intel® FPGA EP3C55F780.

Figure 8 shows the block diagram of this TDC. It consists of a coarse time counter and a fine time measurement stage. The coarse counter is used to record the high bits of the time measurement result, with a clock (CLK_SYS) frequency of 62.5 MHz. The fine time measurement is used to obtain the low bits, with an eight-phase clock (fanned out by an interval phase-locked loop with a 45° phase interval) and a frequency of 375 MHz (equivalent to 3 GHz). The 26-bit coarse counter achieves a measurement range of 1.0737 s, whereas the 6-bit fine measurement

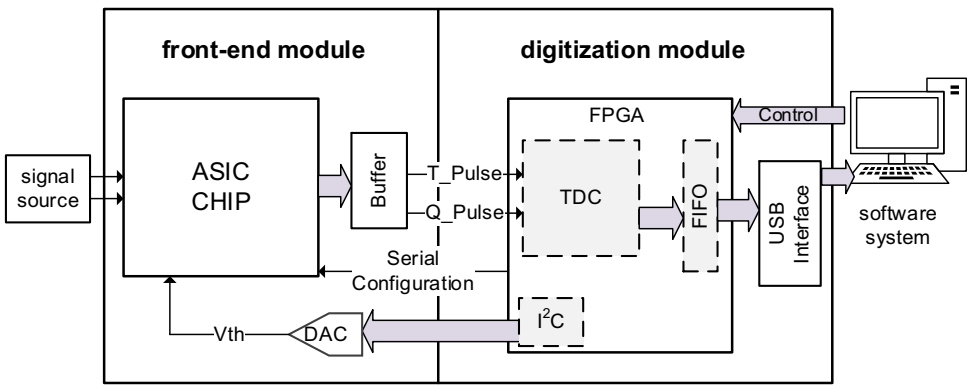


**Fig. 5** (Color online) Block diagram of the test system, mainly consisting of a front-end module, digitization module, and the test software

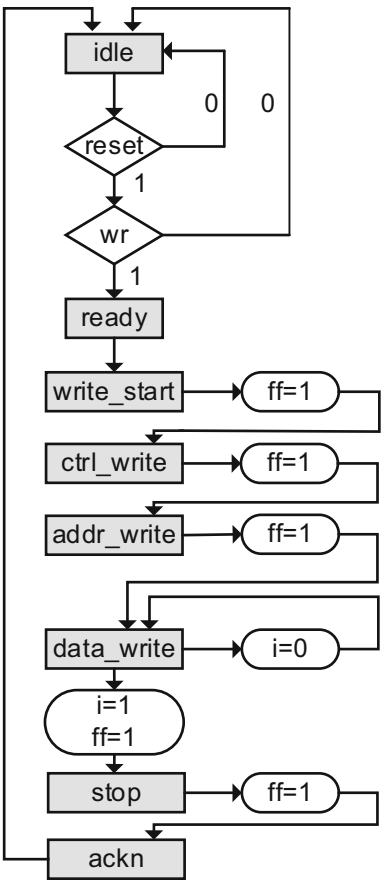


**Fig. 6** ASM figure of $I^2C$ interface

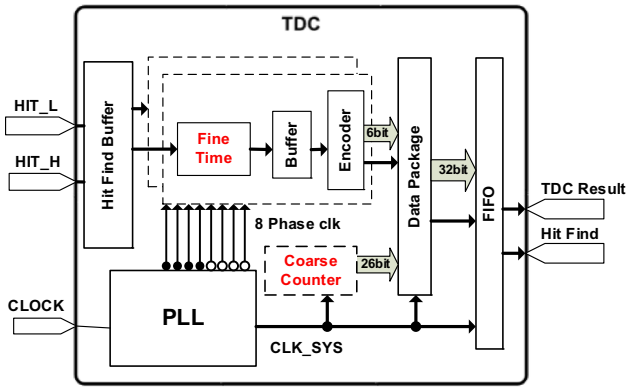


**Fig. 8** (Color online) TDC design in the FPGA, including a 6-bit fine time measurement and a 26-bit coarse counter measurement that constitute a final 32-bit time measurement result (with a 1.0737-s dynamic range and 333-ps bin size)

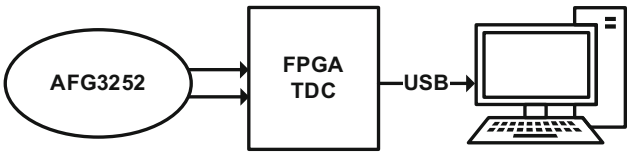


**Fig. 9** TDC test platform setup based on the cable delay test method

corresponds to the TDC bin size of 333 ps. The encoded 6-bit fine time measurement result and the 26-bit coarse counter output constitute a final 32-bit time measurement result, which is read according to first in, first out (FIFO).

Figure 9 shows the tests that were conducted to confirm the functionality and performance of the FPGA-based TDC. The cable delay test method was used [13, 14]. A signal source Tektronix AFG3252 (Beaverton, OR) generates two synchronized output signals (3.3 V CMOS level standard, 10 kHz repetition frequency), which are imported to two TDC channels in the FPGA [15]. By analyzing statistically the time interval of the two TDC channels' output, the time resolution of a single channel can be obtained by dividing the RMS of the time interval by $2^{1/2}$.

Figure 10 shows a typical histogram of time measurement results, with an RMS of 85 ps.

The RMS test results are given as follows: One test result is generated by circuit noise, and the second test results are produced by the quantization error. When the time interval between the two input signals in Fig. 9 changes, the RMS produced by the quantization error varies in a certain pattern, which is well described in Eq. (1) [16].

$$\sigma = T_o\sqrt{c/T_o(1-c/T_o)}, \tag{1}$$

where $T_o$ is the bin size of the TDC, $c$ is the remainder of $T_o$ from time interval, and σ refers to the RMS result.

To accurately evaluate the TDC performance, we changed the time interval and conducted a series of tests (see the results in Fig. 11). A characteristic relationship clearly can be observed, which agrees well with the expected results (marked with a dotted line in Fig. 11). A

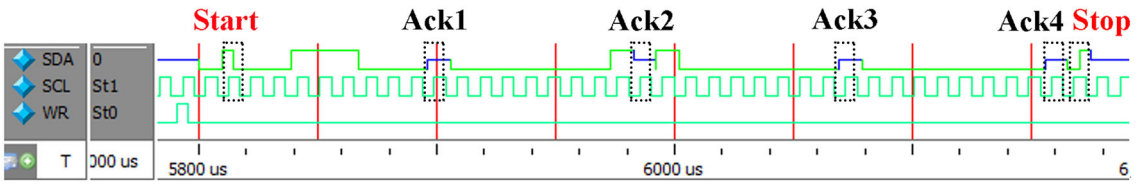


**Fig. 7** (Color online) Simulation result of $I^2C$ timing diagram: SCL (serial clock), WR (write start), and SDA (serial data containing addresses and data). The SCL and SDA communicate on the shared two-wire bus

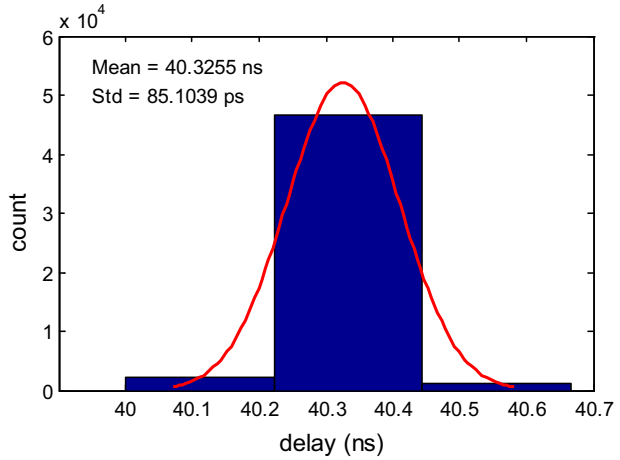


**Fig. 10** (Color online) Normal curve fitting of the test data

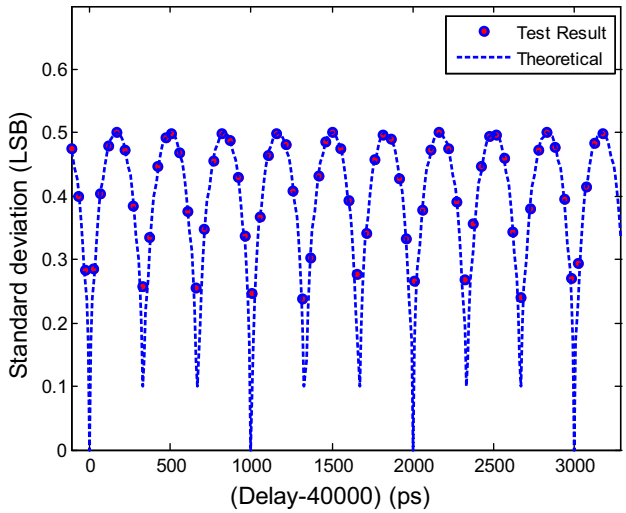


**Fig. 11** (Color online) Eight-phase six-frequency doubling of 62.5-MHz FPGA-based TDC results, plotting the relationship between the RMS and the mean values of the time interval

time resolution (RMS) no worse than 0.5 least significant bits (LSB) is obtained [17].

Characterization of the differential nonlinearity (DNL) and integral nonlinearity (INL) was performed based on the code density test method [18]. Code density is the number of times that every individual code has occurred. When the input signal is not correlated with the TDC clock, with a significant amount of data statistics, the count on each code corresponds to the bin width of that code, and then, the DNL and INL can be calculated. Because each cycle has 48 bins of the CLK_SYS, the nonlinearity is periodic and corresponds to a repeating pattern of every 48 bins. Figure 12 shows the DNL and INL test results which indicate that the DNL and INL are both better than ± 0.2 LSB.

On the basis of this interpolation method, we successfully achieved a high-resolution TDC with a bin size of 333 ps, which is beyond the application requirement. In addition, it has the advantage of low logic resource consumption (469 logic elements per channel) and a large dynamic range (1.074 s) compared with the systems listed in Table 2.

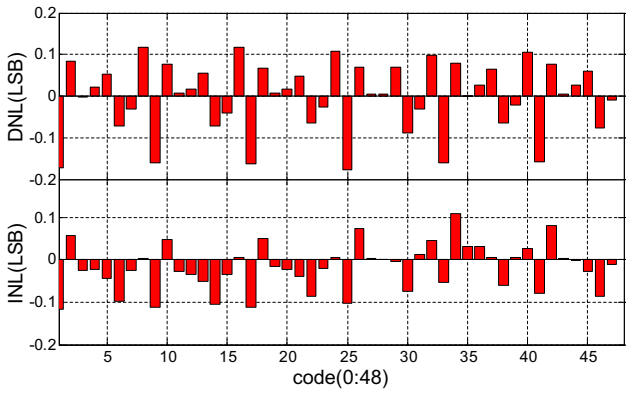


**Fig. 12** (Color online) DNL and INL less than 333 ps FPGA-based TDC. The DNL is in the range of −0.2 to +0.15 LSB, whereas the INL is in the range of −0.15 to +0.15 LSB

### 3.3 USB interface for data readout

A standard USB 2.0 interface is integrated in the test system to transfer the test data to a remote computer. As shown in Fig. 13, a single-chip integrated USB 2.0 transceiver CY7C68013A (Cypress®; San Jose, CA) is used to connect the FPGA and remote PC with a data rate of 240 Mbps. In this work, the chip was programmed as 16-bit data interface, and end-point 2 (EP2) was programmed to transfer the command from a remote PC to the FPGA, and the EP6 was programmed to transfer the test data from the FPGA to a remote PC [19]. A FIFO (1024-word depth, 32-bit input width, and 16-bit output width) was integrated into the FPGA to communicate with the USB. To read out the data through this USB interface, we also designed test software based on Visual C++ (details are presented in Sect. 3.4), with an embedded USB driver.

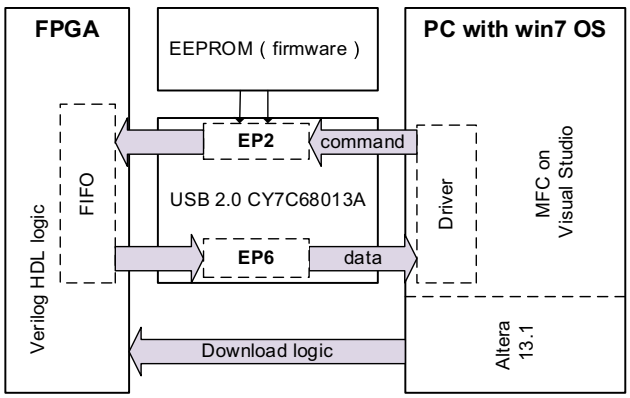


**Fig. 13** (Color online) Block diagram of USB 2.0-based data acquisition

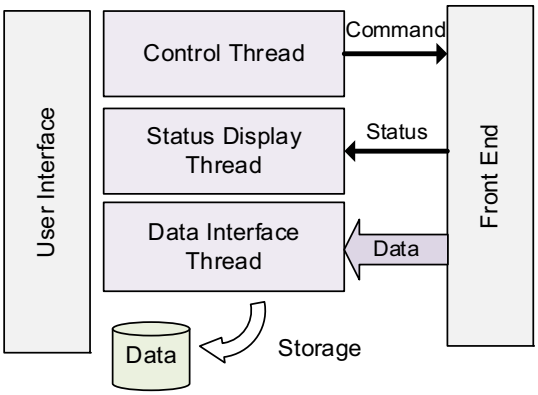


**Fig. 14** Software frame: Three threads are running parallel to achieve data acquisition

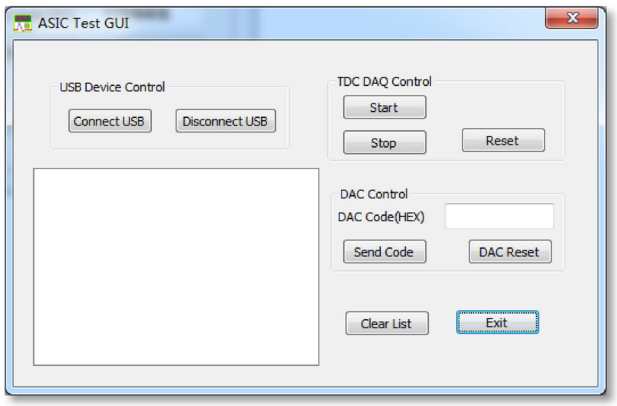


**Fig. 15** Test system GUI

### 3.4 Test software

Figure 14 shows the frame of the software, which contains three independent threads. The control thread sends commands to the FPGA in the digitization module, the status display thread monitors system status in real time, and the data interface thread stores the data to the hard disk.

Figure 15 shows this software's GUI (graphical user interface), which contains all necessary functionalities.

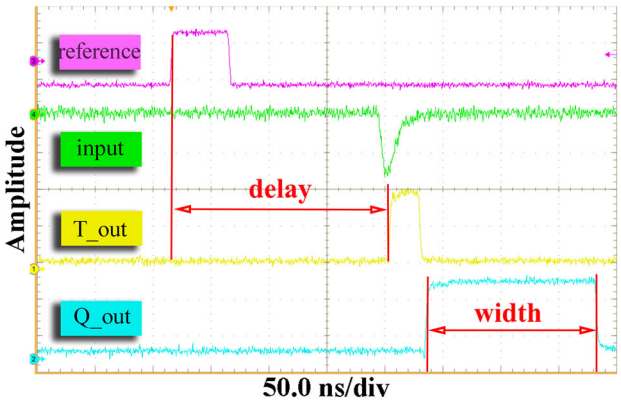


**Fig. 17** (Color online) Waveforms of the ASIC output signals. The reference and input signals are generated by the signal source (Tektronix AFG3252), and the T_out and Q_out signals are the output of the ASIC. The amplitude scale is 700, 50, 100, and 100 mV/div from top down

## 4 Test results

To confirm test system functionality, we conducted tests on real ASICs in the laboratory. Figure 16 shows the test system setup, which consists of a power supply, a signal source (Tektronix AFG3252), an oscilloscope (LeCroy 104 MXi; Chestnut Ridge, NY), and the front-end module and digitization module presented in previous sections.

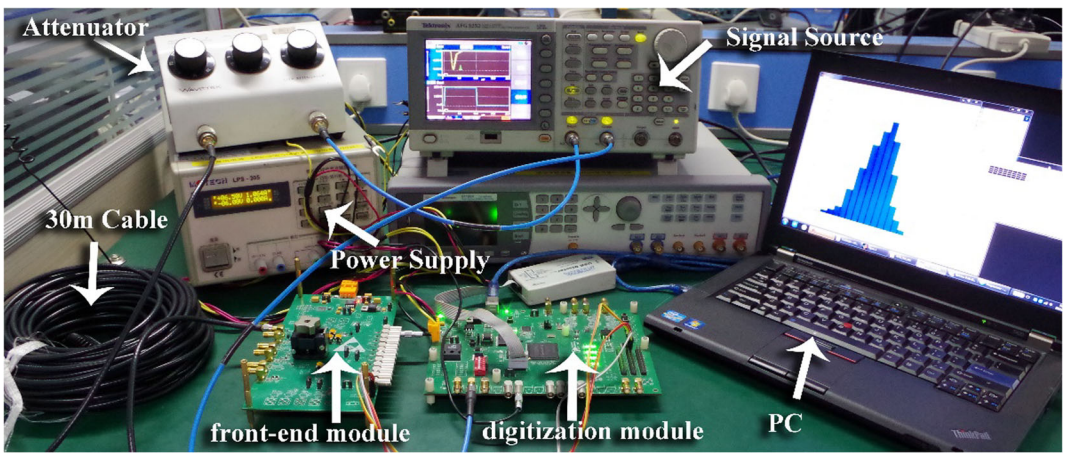


**Fig. 16** (Color online) Test platform of the test system consisted of a front-end module, digitization module, PC, power supply, attenuator, 30-m cable, and signal source

**Table 3** Time measurement results of anode and dynode

| Input amplitude (P.E.) | Low $V_{th}$ | | Input amplitude (P.E.) | High $V_{th}$ | |
|---|---|---|---|---|---|
| | Delay (ns) | Standard of delay (ps) | | Delay (ns) | Standard of delay (ps) |
| 1 | 190.96 | 299.4 | 62.5 | 184.31 | 106 |
| 2 | 189.58 | 232.8 | 125 | 181.9 | 125.6 |
| 4 | 188.43 | 192.3 | 250 | 180.81 | 130.5 |
| 7 | 187.74 | 174.7 | 500 | 180.37 | 113.4 |
| 10 | 187.32 | 161.1 | 1000 | 179.69 | 97.4 |
| 15 | 186.91 | 161.2 | 2000 | 179.3 | 102.1 |
| 20 | 186.61 | 149.1 | 4000 | 178.83 | 136.7 |
| 30 | 186.21 | 161.6 | | | |
| 40 | 185.92 | 152.2 | | | |
| 50 | 185.74 | 149.2 | | | |
| 80 | 185.38 | 137.6 | | | |
| 100 | 185.21 | 161.6 | | | |
| 150 | 184.94 | 140.2 | | | |
| 200 | 184.75 | 145.9 | | | |

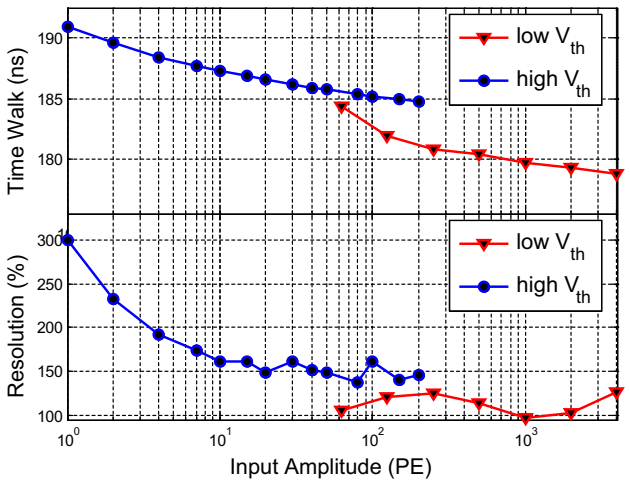


**Fig. 18** (Color online) Time measurement by the FPGA-based TDC with data in Table 3

### 4.1 Functionality test

The ASIC functionality test was conducted by observing the transient waveforms of the critical points of the ASIC using an oscilloscope, as shown in Fig. 17. These waveforms agree well with the ASIC simulation results, which indicate that the ASIC functions well.

In the test, the signal generator outputs two signals. One signal is created by the waveform of the PMT output signal, and it becomes the input signal (in Fig. 17) after passing through a 30-m cable. The second signal is a synchronization signal from the signal generator (i.e., the reference signal in Fig. 17), and a predetermined time interval exists between the input and reference signals. The signal T_out is the output of the ASIC discriminator, whereas the signal Q_out is the output of the QTC. By analyzing the time measurement results between the reference and T_out signals (i.e., the delay in Fig. 17), time measurement performance can be estimated; by analyzing the width of the Q_out signal, charge performance can be obtained. We then conducted a series of tests to evaluate the performance of the ASIC with this test system.

### 4.2 Time measurement result

The time performance test results of the ASIC are shown in Table 3 and Fig. 18.

As shown in Fig. 18, the time walk (i.e., output signal delay of the discriminator compared with the input signal with different amplitudes) is around 10 ns, and the time resolution is more than 300 ps beyond the application requirement. The low $V_{th}$ and high $V_{th}$ refer to test results generated by the discriminator's low (1/4 P.E.) and high (3 P.E. user-controlled) threshold (see Fig. 4). These two thresholds are employed to avoid deterioration of time measurement resolution, which would be caused by noise or interference in the baseline of the large input signal.

### 4.3 Charge measurement results

The charge information of the PMT signals (related to the amount of Cherenkov light) is converted to the width of a pulse signal in the QTC ASIC. By analyzing the digitization output of the FPGA-based TDC, charge measurement performance can be evaluated.

**Table 4** Charge measurement results of anode and dynode

| Input amplitude (P.E.) | Anode | | Input amplitude (P.E.) | Dynode | |
|---|---|---|---|---|---|
| | Width (ns) | Resolution (%) | | Width (ns) | Resolution (%) |
| 1 | 9.27 | 8.4228 | 40 | 8.27 | 8.3761 |
| 2 | 18.54 | 3.9687 | 80 | 16.54 | 4.2086 |
| 4 | 30.52 | 1.9810 | 160 | 30.16 | 2.3203 |
| 7 | 41.09 | 1.2054 | 280 | 42.83 | 1.2727 |
| 10 | 50.13 | 0.9212 | 400 | 53.94 | 0.9282 |
| 15 | 63.73 | 0.6965 | 800 | 85.50 | 0.5185 |
| 20 | 78.6 | 0.5367 | 1600 | 150.29 | 0.2883 |
| 25 | 95.93 | 0.4244 | 2400 | 222.08 | 0.2106 |
| 30 | 115.76 | 0.3550 | 3200 | 300.83 | 0.1711 |
| 40 | 155.76 | 0.2835 | 3600 | 354.64 | 0.1548 |
| 50 | 193.39 | 0.2279 | 4000 | 397.76 | 0.1411 |
| 60 | 225.75 | 0.1985 | | | |
| 70 | 272.88 | 0.1724 | | | |
| 80 | 305.27 | 0.1510 | | | |

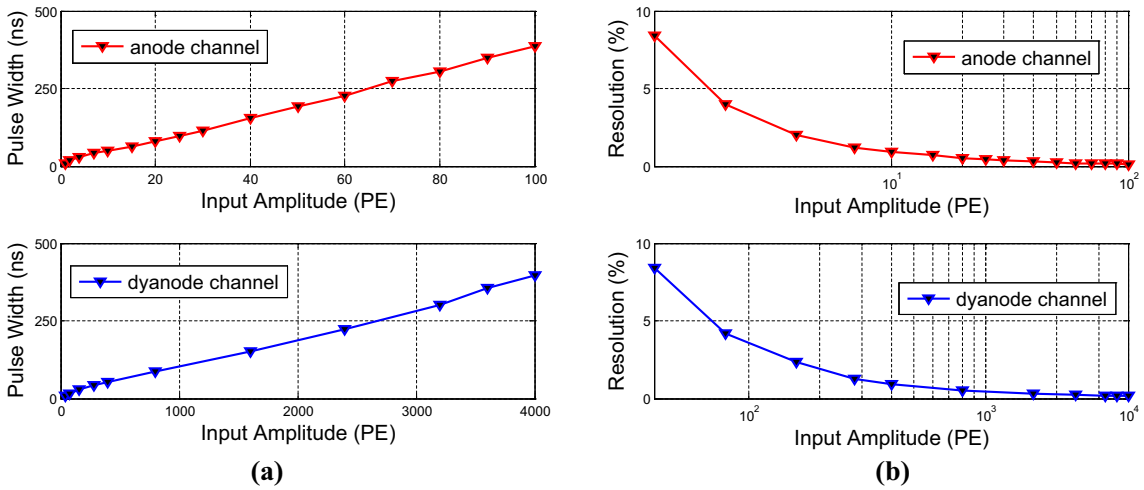


**Fig. 19** (Color online) Charge measurement results by the FPGA-based TDC with data in Table 4. **a** Charge transfer curve, **b** charge resolution

As shown in Fig. 19, by combining the anode and dynode channel, a dynamic range of 1–4000 P.E. is covered, and the charge resolution is better than 10% RMS at 1 P.E. and 1% RMS at 4000 P.E., which are beyond the application requirements.

Using the test system presented in this paper, the ASIC chip designed for the WCDA in LHAASO was tested successfully and demonstrated performance sufficient for this application. With the modular structure of this test system and the design of a general-purpose digitization module, this test system can accommodate different ASIC versions that may be designed in future. In a bulk test of the final 3600 ASICs, multiple front-end modules will be designed, with sockets to mount the ASIC on the printed circuit board without soldering, and each digitization module can be used repeatedly.

### 4.4 Performance comparison

We also investigated the typical ASIC readouts for PMT with a large signal dynamic range and list their performances in Table 5. Compared with these ASICs, the performance test results of our ASIC indicate a larger dynamic range with good time and charge measurement resolution.

**Table 5** Other PMT readout electronic requirements

| | Dynamic range (P.E.) | RMS of time measurement | Resolution of charge measurement (RMS at 1 P.E.) (%) | Quantity of charge (at 1 P.E.) |
|---|---|---|---|---|
| PARISROC [20, 21] | 600 | 1 ns | 30 | 150 fC |
| SPIROC [22] | 2000 | 1.25 ns | 30 | 80 fC |
| SCOTT [23] | 60 | 600 ps | 40 | 8 pC |
| CLC101 [24] | 2500 | 300 ps | 10 | 2 pC |
| ASIC for WCDA | 4000 | 300 ps | 10 | 750 fC |

## 5 Conclusion

A test system was designed to evaluate the performance of a large dynamic range PMT readout for an ASIC designed for the WCDA in LHAASO. The paper presented Kernel parts in the digitization module, including $I^2C$ interface, FPGA-based TDC (333 ps bin size), and USB data interface, as well as the test software. This FPGA-based TDC features low-cost logic resources, wide dynamic range, high precision, and good flexibility. Tests were conducted using this test system to evaluate the real ASIC's performance. Test results indicate that the time resolution is better than 0.5 ns, and the charge resolution is better than 30% RMS at 1 P.E. and 3% RMS at 4000 P.E., which are well beyond the application requirements.

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