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ADC evaluation boards design and test framework for LCLS-II precision receiver

Jin Yang[1,2] · Gang Huang[1] · Qiang Du[1] · Lawrence Doolittle[1] · John Byrd[1]

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Abstract In the low-level RF control field, ADC acquisition accuracy and noise set the boundary of our control ability, making it important to develop low-noise acquisition systems. From the design to test stage, all the noise terms should be understood and characterized. The specific need addressed here is the precision acquisition system for the second Linac Coherent Light Source (LCLS-II), led by SLAC National Accelerator Laboratory. Test circuit boards for the LTC2174 and AD9268 ADCs are designed and fabricated by LBNL. An ADC test framework based on FPGA evaluation board to assess performance has been developed. The ADC test framework includes both DSP (Digital Signal Processing) firmware and processing software. It is useful for low-level RF control and other synchronization projects. Investigating the clock jitter between two channels give us an understanding of that noise source. Working with the test framework, the raw ADC data are transferred to a computer through a Gigabit Ethernet interface. Then short-term error signal can be calculated based on a sine wave fit. By changing low-pass filter bandwidth, relative long-term performance can also be obtained. Amplitude jitter and differential phase jitter are the key issues for ADCs. This paper will report the test results for LTC2174 and AD9268 chips. The integral amplitude jitter is smaller than 0.003 %, and the integral phase noise is smaller than 0.0015° (measured at 47 MHz RF, 100 MHz clock, bandwidth 1 Hz to 100 kHz) for both ADC chips.

Keywords Precision acquisition · LLRF · LTC2174 · AD9268 · ADC · Framework

1 Introduction

LCLS was the world's first hard X-ray-free electron laser [1]. The follow-on project known as LCLS-II plans to provide up to 1 million pulses per second, rather than the 120 pulses per second from the original LCLS project. The project upgrades the whole accelerator system with a 4 GeV CW superconducting linac. Thirty-five TESLA-ILC 1.3 GHz style cryomodules will be installed. The relatively high loaded Q (4×10^7) leads to 16 Hz half-bandwidth [2]. This narrow bandwidth combined with microphonic detuning poses a difficult control task for cavity resonance control and field control. But at the same time, the integral noise in the system bandwidth will be very small. The field detection will be relatively easier.

The low-level RF control system is tasked with holding the cavity field stable to 0.01 % and 0.01° rms. From the experience in Lawrence Berkeley National Laboratory (LBNL), detecting and controlling the field as specified is possible, but gets close to the hardware limitations [2–6].

LBNL used the LLRF4 board for many synchronization projects. Its control ability is limited mostly by the board's ADCs. Based on the experience from the LLRF4 board, ADC evaluation boards are designed for LCLS-II precision receiver chassis. One board is for LTC2174 [7], the other is

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✉ Gang Huang
ghuang@lbl.gov

[1] Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA

[2] Department of Engineering Physics, Tsinghua University, Beijing 100084, China

for AD9268 [8]. The purpose of using LTC2174 is try to use the high-speed serial data acquisition. AD9268 has the relative high signal-to-noise ration (SNR) 78.2 dBFS (Fig. 1).

2 Hardware design

Two separate ADC test boards are designed by LBNL. One board is for LTC2174, the other is for AD9268. The two boards are shown in Fig 2.

One board is using the 14-bit/4-channel/105 Msps LTC2174 chip. This chip claims 73.1 dB SNR and 88 dBc spurious-free dynamic range (SFDR). it is configured in two-lane output mode, and 14-bit data for each channel can be sent by the chip through two low-voltage differential signaling (LVDS) pairs. This high-speed serialization feature reduces pin count, which is an important factor when designing a ADC mezzanine card and selecting an FPGA package. It takes 10 pairs (8 pairs for data output, 1 pair for FRAME, 1 pair for DCO) of LVDS pins for four channels of data acquisition, and four low-voltage complementary metal oxide semiconductor (LVCMOS) pin for serial peripheral interface (SPI) control. The ADC has good performance and saves data pins. But it takes effort to deal with the high-speed serialized data output interface. We succeeded in using the Spartan-6 ISERDES [12] to receive the high-speed serialized data.

The AD9268 chip has higher SNR of 78.2 dB and almost the same SFDR 88 dBc. Using the AD9268 is for the higher-precision measurement. It take 18 pairs of LVDS pins for acquiring two channels, and three LVCMOS pins for SPI control. On the driver side, the task is to take care of the SPI control part. The Double Data Rate (DDR) data acquisition logic is comparatively easier. The performances of the two ADCs are summarized in Table 1.

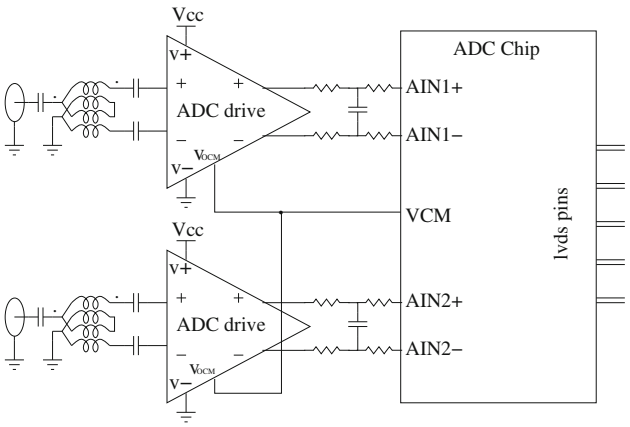


Fig. 1 ADC test schematic design

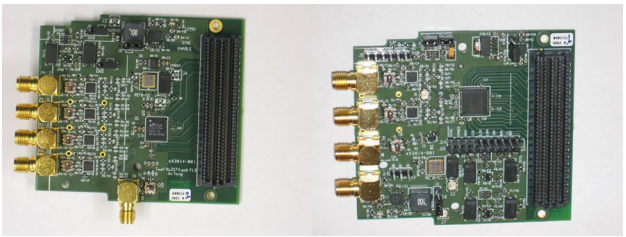


Fig. 2 LTC2174 and AD9268 boards

Table 1 ADC spec

Part no.	AD9268	LTC2174
Num of bits	16	14
Sampling rate (Msps)	105	105
ADC SNR@30MHz (dB)	78.2	73.0
p-p full scale (V)	2.00	2.00
FPGA pins per channel	17	5
Num of channels	2	4

In this design, the LTC6401 [9] ADC driver chip is used in the signal conditioning path. Its common-mode voltage output range is from 1.0 to 1.5 V. But the common-mode voltage output from the ADC should be around 0.9 to 1.0 V. This is a small defect, but the system still works. The next time to use an ADC driver chip, the common-mode range should be carefully chosen.

An ultra-low noise 1.8 V power supply is made up of an LTC6655 precision voltage reference chip, an op-amp, and a transistor. The noise floor above 100 Hz is $5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, much cleaner than commercial LT1763-1.8 ($40\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$) [10]. In the 0.1 Hz to 10 Hz range, with careful design, $1/f$ noise is measured as expected. There are two jumper-selectable 1.8 V analog power supplies on the AD9268 board, allowing us to characterize ADC performance with either the custom ultra-low-noise supply or a simple LT1763-1.8. Not much difference is observed, although experiments are continuing.

3 Firmware and software

The test system is based on the SP601 Spartan-6 Evaluation board [11]. Utilizing the general-purpose Ethernet/IP/UDP (User Datagram Protocol) engine developed by LBNL, the boards can communicate at high speed to a commodity workstation.

Figure 5 shows the simplified ADC test setup and the framework of the FPGA firmware. On the firmware side, it takes lots of effort to deal with the ISERDES clocking resources (especially bank restrictions) and bitslip. This is the most difficult part of our driver development. Figure 3

shows LTC2174 driver diagram. Figure 4 shows AD9268 driver diagram. The remaining DSP part is same for the two chips, and is based on the logic used in low-level RF control (LLRF). The DSP part is composed of mixer, direct digital synthesizer (DDS), local oscillator (LO) generator, and CORDIC [13] module. After implementing DSP module, the amplitude/phase data can be sent to a CIC low-pass filter. The averaging length of the low-pass filter can be configured from 1 to 2^{29}, so that the noise spectra can be characterized down to 0.01 Hz. Using a set of external triggerable circular buffers, the selected waveforms will be recorded simultaneously. Then the data will be transmitted over Ethernet as UDP packets read by PC side software.

On the software side, python script is used for board configuration and data acquisition. For each test board, a class is created which is implemented with board operation and raw data conversion. The base class 'adc_board' is developed for general-purpose ADC data processing. The important functions in the class are listed in Table 2.

The general-purpose 'adc_board' class is mostly for data processing. The spectrum can tell whether there is any abnormal noise. The phase noise and amplitude noise density can tell the phase and amplitude detection ability of the ADC board. To test the LTC2174 and AD9268, two classes are derived from the 'adc_board' class. Most of the functions in the derived class are for board communication, board setting, and buffers operation as listed in Table 3.

The general setting and buffer operation details are in the derived classes. For a new ADC board, general setting and buffer operations need to be implemented in the derived class. The DSP module in FPGA firmware and the 'adc_board' class can still be used without modification. The 'DSP' module in FPGA firmware, and 'adc_class' in python code are the cores of the ADC test framework.

4 DSP algorithm

The digital signal processing chain is based on low-level RF signal processing using non-IQ sampling [15]. The input signal is mixed with local oscillator signal, then goes through a cascaded-integrator-comb (CIC) filter to get the I/Q component. Then a CORDIC module converts I/Q to amplitude/phase. Then processing data gets sent to buffers directly or through a low-pass filter as shown in Fig. 5.

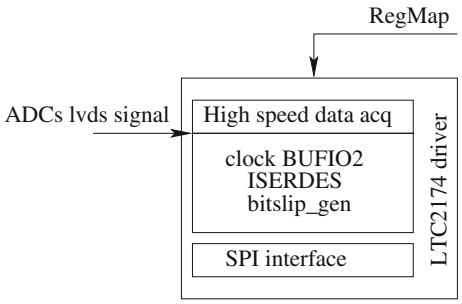


Fig. 3 LTC2174 driver

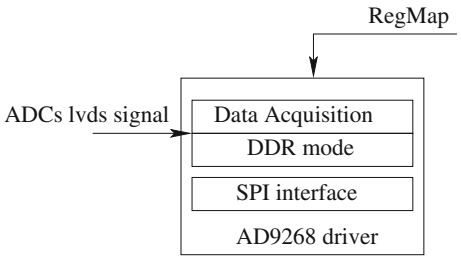


Fig. 4 AD9268 driver

The 'local oscillator generator' or DDS is composed of a phase accumulator and a CORDIC module. The structure of this DDS is shown in Fig. 6. The CORDIC module is supplied with accumulated phase and a fixed amplitude, and the subsequent sin and cos signals are generated by the CORDIC module. This kind of DDS is flexible. The LO frequency can be changed by simply adjusting the 'phase_step' register.

The mixer is just a multiplier. In this case the ADC signal inputs to the multiplier is 16 bits signed (for a 14-bit ADC, two zeros are appended after the least significant bit, LSB). The LO signal to the multiplier is 18 bits signed.

$$\frac{(1-z^{-R})^N}{(1-z^{-1})^N} = \left(\sum_{k=0}^{R-1} z^{-k}\right)^N \tag{1}$$

In Eq. 1, R is sampling rate change factor and N is the number of cascaded-integrator-comb stages. In the test, $N = 2$ is set for I/Q CIC filter. $N = 1$ is set for the amplitude and phase CIC filter. R for both CIC filters can be configured through the python script.

In LLRF and synchronization systems, the dominant performance metrics are the amplitude and phase noise spectra. By changing the sampling rate factor R for the amplitude/phase CIC filter, and sending the filtered data to buffers, the noise in different frequency bands can be investigated. For amplitude noise, it can be derived from the discrete Fourier transformation of amplitude data directly [16]. For phase noise, the single side band phase jitter density spectra $\phi_{\text{jitter\_density}}$ also can be derived from the discrete Fourier transformation of phase data directly. Based on Eq. 2, the general phase noise density function $L(f)$ can be calculated [17] in 'dBc/Hz'. In Eq. 2, the unit of $\phi_{\text{jitter\_density}}(f)$ is 'rad/$\sqrt{\text{Hz}}$'. The integral phase jitter $\phi_{\text{jitter}}(f)$ can be derived from Eq. 2. The performance of these two ADC chips is shown in the next section.

Table 2 adc_board class

Function	Description
read_buf_data	Read buffers data and raw data decoding; Utilize the buf_read() from the derived class
buf_skip	Skip the buffer data
buf_wait	For different low pass filter averaging length, Wait for different time for buffer filling time
get_adc_data	Plot or save raw adc data to file, length=1024
get_amp_info	Plot or save amplitude information, length=1024
get_phase_info	Plot or save phase information, length=1024
plot_buf_data	Plot real time waveforms: (1) ADC raw data; FFT spectrum; sine fit; (2) Amplitude information for two channels; (3) Phase information for two channels;
sine_fit	Sine wave fit function
histogram	Shorted input histogram and sine wave fit error histogram
plot_hist	Plot the histogram
fft_db	Data spectrum analyze
plot_fft_avg	Plot fft spectrum with averaging ability
phase_noise_density	Plot phase noise density same as signal source analyzer does;
amp_noise_density	Plot amplitude noise density

Table 3 Functions in derived class 'app_ltc2174/app_ad9268'

Function	Description
reset	Reset ADC board to default setting
registers	Set registers in FPGA
buf_mode	Select which data is sent to buffers
buf_trig	Trigger buffers to record input waveforms
buf_read	Read buffer data back
set_lpf_length	Set averaging length for low pass filter
set_trig_internal	Internal/external trigger selection

$$L(f) = 20\log(\phi_{\text{jitter\_density}})$$
$$\phi_{\text{jitter}}(f) = \sqrt{2 \times \int 10^{L(f)/10} \cdot \mathrm{d}f} \quad (2)$$

5 Test result

The test system setup is shown in Fig. 7. An Agilent 33600A Series Waveform Generator is used for the 100 MHz sampling clock generation. A Berkeley Nucleonics Model 845 RF signal generator generated the 47 MHz RF signal fed to the ADCs.

First, the ADC raw data and sine fit result are shown here. Figure 8 shows the raw ADC data and sine curve fit for LTC2174. Figure 9 is for AD9268 sine fit. The 14 bits of ADC data for LTC2174 is padded to 16 bits by adding two zeros at the end. The maximum ADC count is about 25000, or −2.3 dBFS. This is representative of real LLRF system use, where some control and operability margin needs to be included in the RF chain setup.

Figure 10 shows the histogram of fitting errors @16 bits for LTC2174. The RMS fitting error is 3.4 LSB@16 bits or 1.4 LSB@14 bits for LTC2174 channel 1. Figure 11 shows the fitting error histogram for AD9268. The RMS fitting error is 3.2 LSB_{rms} error for AD9269 channel 1.

Figure 12 shows the LTC2174 channel 1 measured amplitude information. Figure 13 shows the AD9268 channel 1 measured amplitude information. The amplitude information are from 'amp1' shown in Fig. 5 directly. The only filter applied on the amplitude information is the I/Q CIC filter ($R = 100$, $N = 2$). In this short-term measurement (1 ms), the RMS amplitude jitter is smaller than 0.01 %. Much more details are shown in the integral amplitude noise figures.

Figure 14 shows single side band amplitude noise density for the two ADCs. The other side band noise power need to be taken into account for the integral noise calculation. It means that the noise power need to be doubled for noise integration. The noise measured by the ADCs is composed of RF signal generator noise, the drive amplifier noise, and the noise from the ADC itself. The effect of 2 stages CIC filter can be seen from 100 kHz to 500 kHz in

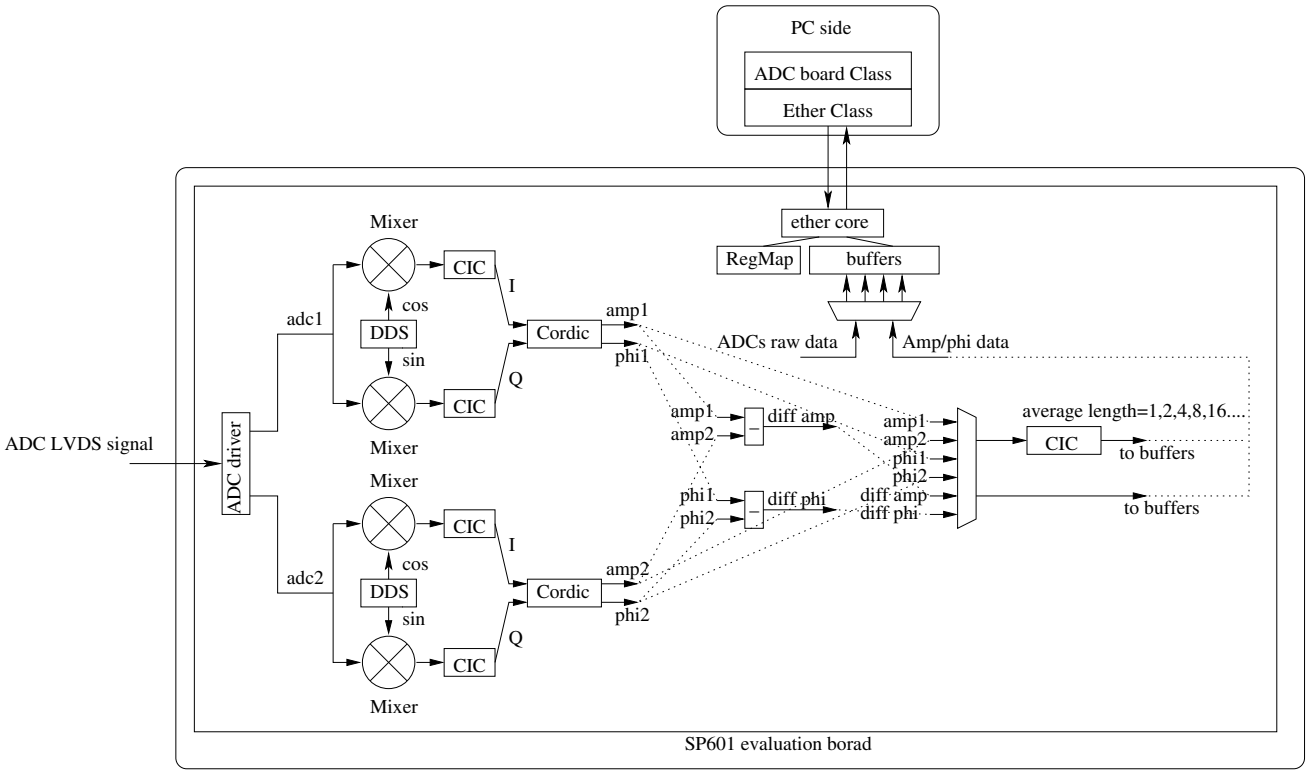


Fig. 5 ADC test diagram

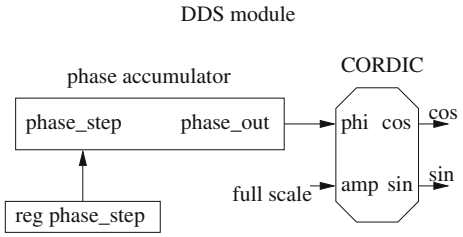


Fig. 6 DDS module structure for LO signal generation

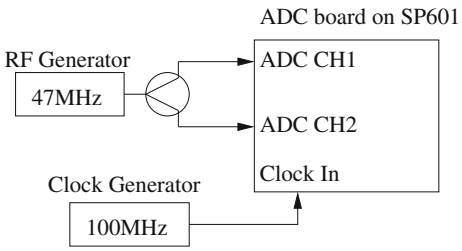


Fig. 7 ADC test setup for additive phase noise and amplitude noise measurement

this figure. Without CIC filter the noise floor should be flat. Computations show that the CIC filter will affect the test result by not more than 5 % below 200 kHz. The result below 200 kHz should be trustworthy.

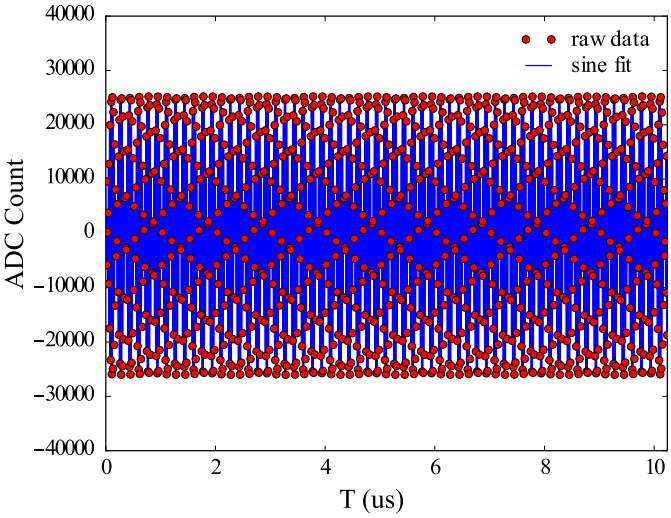
Figure 15 shows the integral amplitude noise from 1 Hz to 500 kHz. It can be implied from this figure that how much noise will this kind of amplitude detector adds. And the control ability can be roughly predicted. For the LCLS-II Superconducting cavity, the cavity bandwidth is smaller than 100 Hz, so the amplitude detection RMS additive noise generated by ADC from 1 to 100 Hz should be lower than 0.001 %. The integral amplitude noise figure implies that the performance of LTC2174 and AD9268 are similar in the low frequency range (1 Hz to 1 KHz). This may result from the RF signal source itself. In the relative high frequency range (1–500 kHz), performance of amplitude detection for AD9268 is better than for LTC2174. The conclusion is that even in 0.01 % amplitude control system, a 14-bit ADC is still suitable.

After showing the amplitude detection ability, here shows the phase detection ability. Figure 16 shows the differential phase noise density between two channels. Figure 17 shows the two channels differential phase of AD9268. Compared with real LLRF control board, in this experiment, the result is free from the additive noise from clock distribution chip, for example an AD9510. The result in this paper will show the limitation of the phase detection ability. This test framework is still applicable for the performance test between two chips.

As is in amplitude result part, showing the noise density and integral noise will give the detail information for phase detection ability.

Figure 18 shows the phase noise spectrum of the differential phase. Figure 19 shows the integral phase noise.

Fig. 8 1k points LTC2174 ADC1 raw data and sine fit



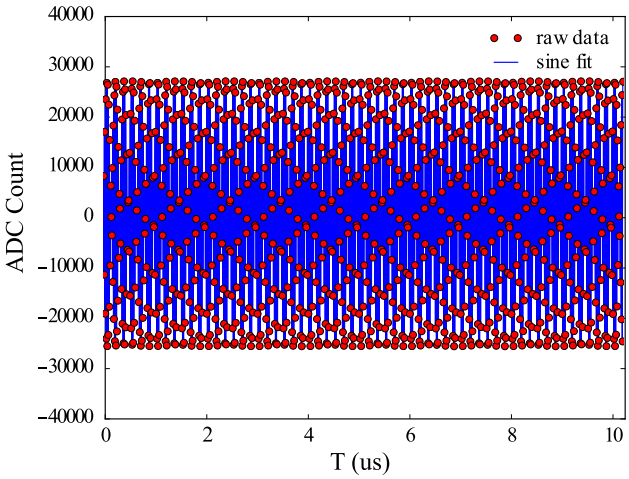


Fig. 9 1k points AD9268 ADC1 raw data and sine fit

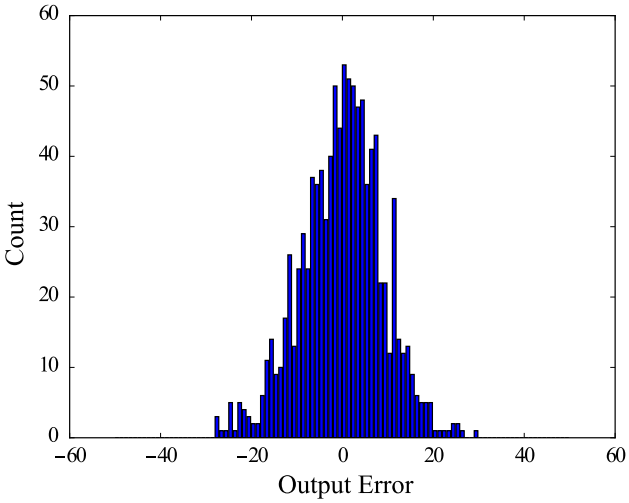


Fig. 11 1k points AD9268 ADC1 sine fit error histogram

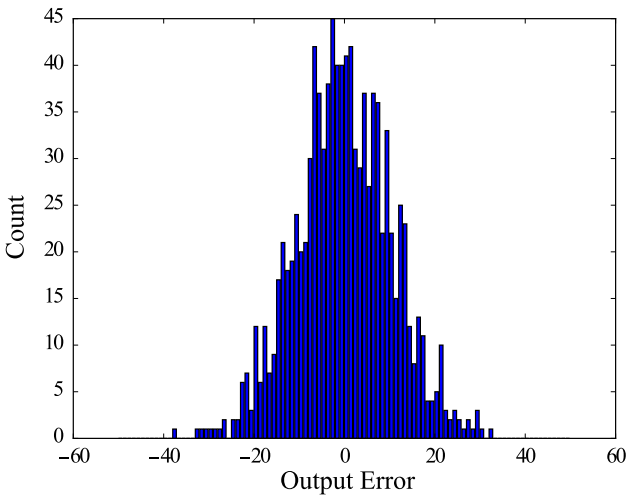


Fig. 10 1k points LTC2174 ADC1 sine fit error histogram

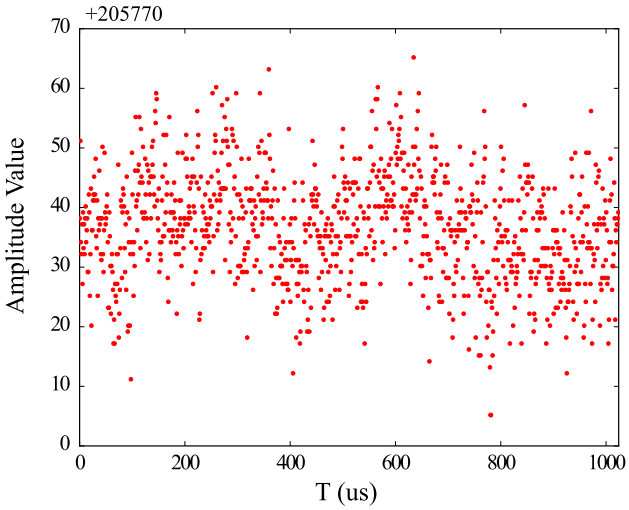


Fig. 12 The amplitude value of 47 MHz signal measured by ltc2174 channel 1

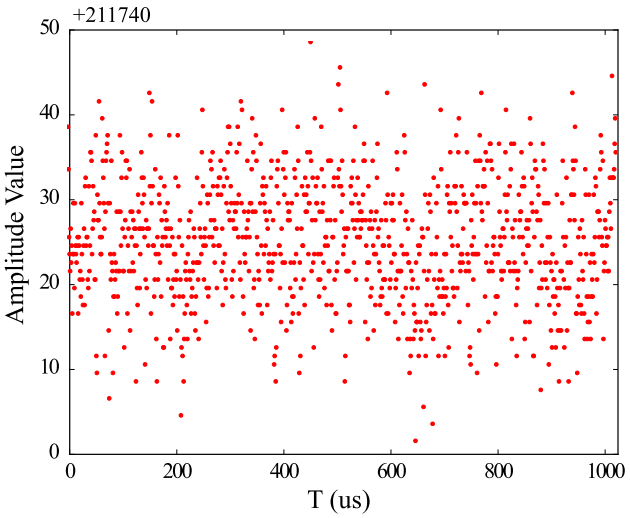


Fig. 13 The amplitude value of 47 MHz signal measured by ad9268 channel 1

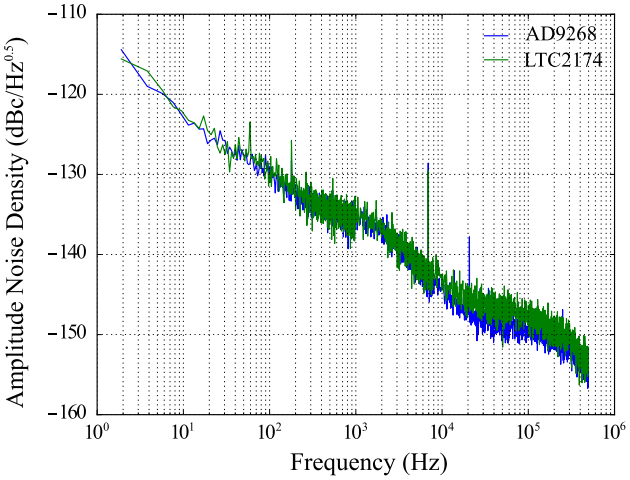


Fig. 14 The 47 MHz signal amplitude noise density measured by ltc2174/ad9268 boards, respectively

The phase detection performance for AD9268 is better than LTC2174. From 1 to 100 Hz, the integral phase jitter is smaller than 0.0003° which is much better than the requirement. The integral phase jitter from 1 Hz to 100 kHz is smaller than 0.0015°. This result tells us, if the interested bandwidth is smaller than 100 kHz, it is possible to get sub-10-femtosecond control ability or even better. This feature is very important for phase reference distribution system. The Phase averaging reference line based on digital LLRF structure will be suitable for sub-10-femtosecond synchronization.

The performance may be limited by the ADC drive chip. Designing a board without an active device may tell us the real detection ability.

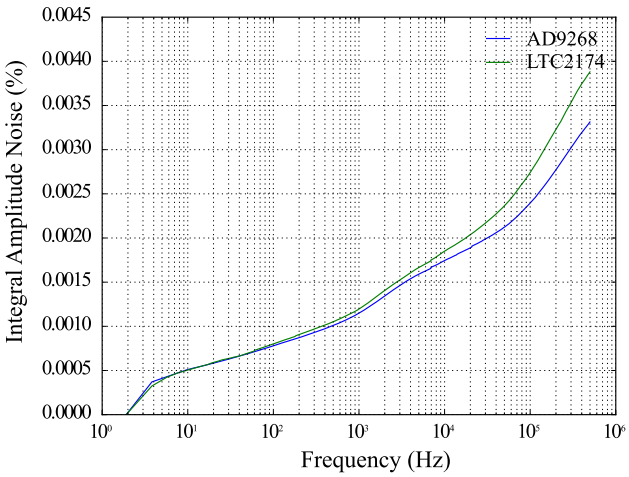


Fig. 15 Integral amplitude noise of 47 MHz signal measured by ltc2174/ad9268 boards, respectively

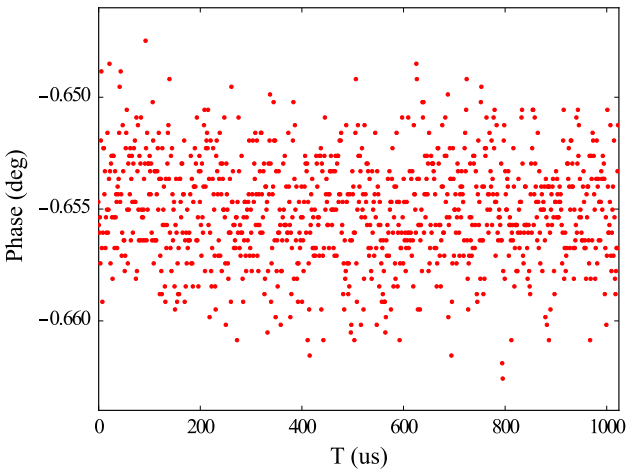


Fig. 16 The measured phase difference between channel 1 and channel 2 for ltc2174 board when measuring 47 MHz signal

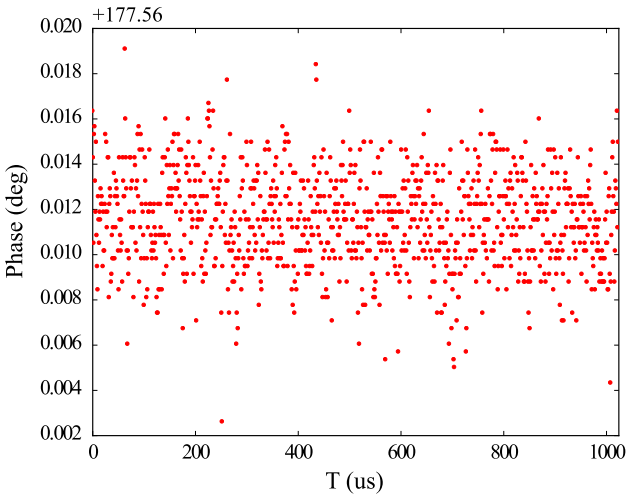


Fig. 17 The measured phase difference between channel 1 and channel 2 for ad9268 board when measuring 47 MHz signal

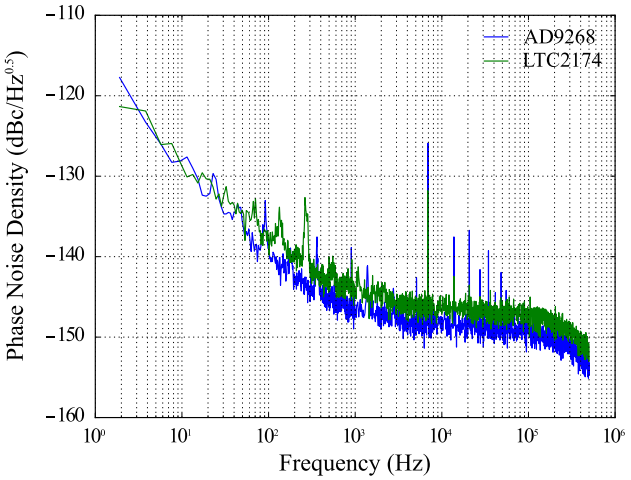


Fig. 18 The measured differential phase noise density for ltc2174/ad9268 boards respectively when measuring 47 MHz signal

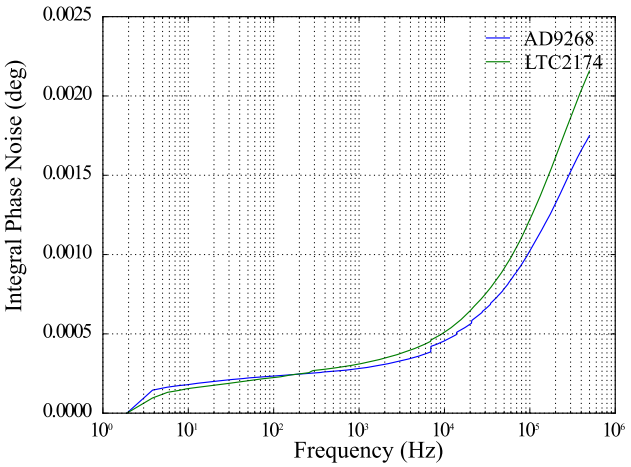


Fig. 19 The integral differential phase noise for ltc2174/ad9268 boards respectively when measuring 47 MHz signal

6 Conclusion

The ADC test framework can measure the crucially important amplitude and phase spectrum of an ADC board. Using the framework as implemented here will give a fast evaluation of the ADC performance.

These LTC2174/AD9268 boards show excellent amplitude and phase detection ability. These two ADCs both satisfy the core LCLS-II LLRF control requirements. The RMS amplitude noise is smaller than 0.003 % (integral from 1 Hz to 100 kHz). And the 0.0015° phase noise (integral from 1 Hz to 100 kHz, 47 MHz RF, 100 MHz clock) really seems adequate for phase ultra-low-noise distribution, LLRF control and laser oscillator synchronization.

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