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Development of the bunch-by-bunch beam position acquisition system based on BEEcube

Yong Yang[1,2] · Yong-Bin Leng[1] · Ying-Bing Yan[1] · Wei-Min Zhou[1] · Ren-Xian Yuan[1] · Zhi-Chu Chen[1]

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Abstract In this paper, we report the development of a bunch-by-bunch beam position acquisition system. Through a wideband synthesizer of PLL, the system realizes synchronous clock of bunch signal. Based on the high-performance FPGA hardware DAQ environment, four-channel raw data of beam signal can be achieved. Test results in the SSRF storage ring show that the system can obtain beam position of single bunch with the resolution of 10 μm and multi-bunch instability can be observed.

Keywords Bunch by bunch · BPM · FPGA · SSRF

1 Introduction

Beam diagnosis system, with which many accelerator parameters can be obtained, is essential for an accelerator system [1–3]. For achieving high current, high brightness and favorable stability of a synchrotron light source, beam bumps in the storage ring should be monitored in real time. Beam instability, which can be affected by wakefield, transverse coupling, ion trapping, etc., will depress the beam quality or even cause beam lost [4–6].

Measuring the bunch-by-bunch position helps studying the beam impedance, coupling instability and nonlinear dynamics quantitatively and provides an powerful tool to study accelerator physics [7–9]. In this paper, we report details of the bunch-by-bunch beam position measurement system and the results of beam experiment.

✉ Yong-Bin Leng
lengyongbin@sinap.ac.cn

[1] Shanghai Institute of Applied Physics, Chinese Academy of Sciences, Shanghai 201800, China

[2] University of Chinese Academy of Sciences, Beijing 100049, China

2 Measuring principle and requirement analysis

Using four button electrodes as beam position monitor (BPM), neglecting higher order terms, four-channel-induced voltage signals can be expressed by Eq. (1) when one electron-beam bunch passes through the BPM [10, 11].

$$\begin{cases} V_{\mathrm{A}}(t) = V_o(t)(1 + \alpha x + \beta y) \\ V_{\mathrm{B}}(t) = V_o(t)(1 - \alpha x + \beta y) \\ V_{\mathrm{C}}(t) = V_o(t)(1 - \alpha x - \beta y) \\ V_{\mathrm{D}}(t) = V_o(t)(1 + \alpha x - \beta y) \end{cases} \quad (1)$$

where, $V_{\mathrm{o}}(t)$ is the BPM signal when the beam is in the center of the BPM detector; x and y denote the position at which the beam bunch passes the BPM; α and β are constants relevant to mechanical dimension of the BPM, and the subscripts A–D denote the four channels. Figure 1 shows a typical waveform of the induced voltage signal.

Sampling the four voltage signals simultaneously, and eliminating the common factor $V_{\mathrm{o}}(t)$, one has Eq. (2) to calculate the beam bunch position (x, y):

$$\begin{cases} x = k_x \cdot (V_{\mathrm{A}} - V_{\mathrm{B}} - V_{\mathrm{C}} + V_{\mathrm{D}})/(V_{\mathrm{A}} + V_{\mathrm{B}} + V_{\mathrm{C}} + V_{\mathrm{D}}) \\ y = k_y \cdot (V_{\mathrm{A}} + V_{\mathrm{B}} - V_{\mathrm{C}} - V_{\mathrm{D}})/(V_{\mathrm{A}} + V_{\mathrm{B}} + V_{\mathrm{C}} + V_{\mathrm{D}}) \end{cases}, \quad (2)$$

where k_x and k_y are constants relevant to the mechanical dimension of the BPM.

Considering the signal-to-noise ratio (SNR), the ideal sampling point is at the waveform peak. If the sampling

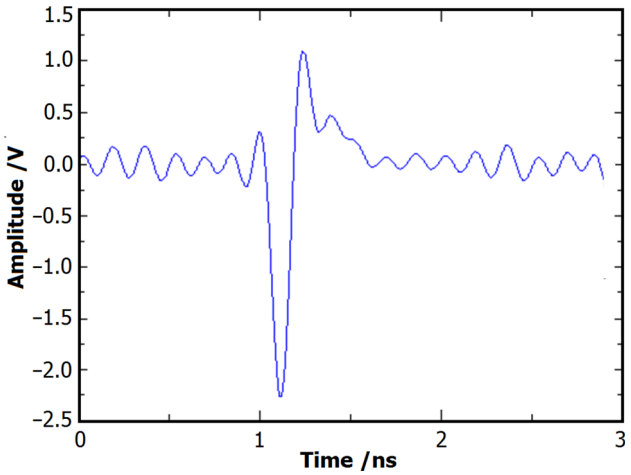

Fig. 1 Typical waveform of the induced voltage signal

point is at the zero-crossing point of the signal or too far away from the peak, only noise is sampled [12].

The RF frequency of SSRF is 499.654 MHz [13], which means a 2-ns interval between two consecutive bunches, hence the sampling rate of 499.654 Msps (million samples per second) at least for the bunch-by-bunch beam position acquisition system.

Any two-clock source will cause phase error in a long period of time even their nominal frequencies are the same [14], so the sampling clock drives the acquisition system must be synchronous with the bunch to ensure the fixed sampling point relative to the bunch bucket.

To observe the damping phenomena of betatron oscillation (about 5–6 ms in SSRF) [15], the data buffer of the acquisition system must be large enough to acquire data longer than 6 ms (>3 Mpts) continuously. Of course, the greater the number of points, the more the new physical phenomena can be discovered.

3 Design and realization of the system

3.1 Hardware setup

The hardware architecture of the bunch-by-bunch beam position measurement system is shown in Fig. 2.

To get the synchronous sampling clock, we use a wideband synthesizer of PLL (phase-locked loop) to multiply the machine clock (694 kHz at SSRF) to 720 times [16]. Since the machine clock is synchronous with the electron-beam bunch train, the sampling clock shall be synchronous with the electron-beam bunch train too. There are 720 buckets in the storage ring, so each period of the sampling clock corresponds to one bucket [17]. And the frequency of sampling clock is strict equal to RF frequency.

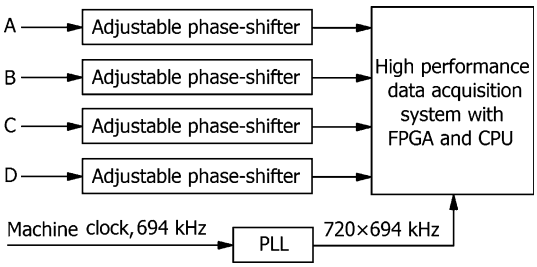

Fig. 2 Hardware architecture of the bunch-by-bunch beam position measurement system

The data acquisition system has four channels and works at the sampling rate of 499.654 Msps at least. And, for better resolution of the position measurement, its ADCs should have enough binary digit bits. Based on these considerations, we choose BEEcube as data acquisition system. BEEcube is a high-performance FPGA-based computing, prototyping and emulation platform, featuring the Xilinx Virtex-6 family of FPGAs. The system also integrates Intel i7 CPU and installs operation system (Linux) on it. 4 GB DDR3 module on board is large enough to capture over 10 Mpts of raw data (about 20 ms). The ADC is ISLA214P50, a 14-bit 500 Msps ADC designed with a standard CMOS process. This ADC utilizes two time-interleaved 250 Msps unit ADCs to achieve the ultimate samplING rate of 500 Msps, so its quantization bits are greater than most existing ADCs of 500 Msps.

The cables from BPM to each channel of the data acquisition system may differ a little in length, so an adjustable phase shifter is used for each channel to have the sampling point at the peak of signal waveform. The best adjustable time delay extent is 2 ns. If it is over 2 ns, sampling bunches of the four channels would be different; while if it is too small, the sampling point would not be adjusted at the waveform peak.

3.2 FPGA logic design

Based on BEEcube Platform Studio, a logic module is implemented within the FPGA as the data transfer and control among ADC, DDR3 memory and CPU. The logic design in FPGA is shown in Fig. 3.

The ADC interface receives the data stream from ADC of 500 Mbps (million bits per second) data rates. The speed of FPGA internal logic processing cannot reach 500 MHz, so the ADC interface uses serial-to-parallel conversion method to reduce the data rate to 250 Mbps.

The DDR interface module has an asynchronous 1:2 FIFO and an interface layer of the Xilinx DDR3 memory controller. The asynchronous 1:2 FIFO, between other logic and the memory controller, allows the system clock to run at any arbitrary frequency independent of the

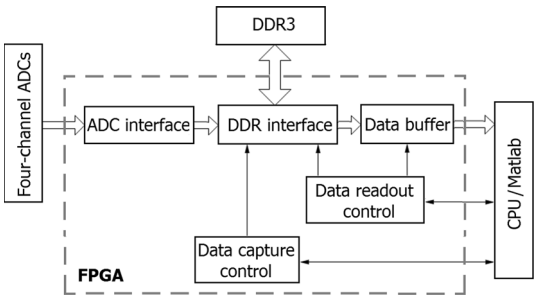

Fig. 3 Logic design in FPGA

memory clock. Independent FIFOs are used for address requests, write data and read data with flow control and DDR3 commands handled automatically by the underlying logic. The data FIFOs is of 128 bits. Since the BEEcube memory configuration uses a 64-bit datapath (72-bit ECC DIMMs) and the DDR3 burst length is set to 8 cycles (the ideal setting), each transaction consumes 512 bits of data, which equates to 4 cycles worth of FIFO data at 128 bits per cycle. Therefore, with a DDR3 burst length of eight, four cycles of data must be pushed into the write FIFO (or popped from the read FIFO) for each address request. To make sure that the number of commands issued on the address request FIFO is kept in synchronization with the amount of data read/written on the data FIFOs, a counter with enable port is used as the address generator.

The data capture control module interprets the data capture command from CPU to a pulse signal, and this pulse signal informs the DDR interface to capture data from ADC interface and saves data to DDR3 memory connected to the FPGA.

The data buffer module is provided by BEEcube Platform Studio. With data buffer module, data can be interchanged between FPGA and CPU.

The data readout control module interprets the data readout command. It informs the DDR interface to read data from DDR3 memory and controls the data buffer module to receive data from DDR interface.

3.3 Data interchange between FPGA and CPU

The BEEcube Platform Studio provides two methods for data interchange between FPGA and CPU. One is 'software register,' which can be used to access single 32-bit data values in both hardware and software. It can be written by the processor (acting as an input to the FPGA design), or be read by the processor (acting as an output from the FPGA design). Figure 4a shows the 'write software register.' The 'sim_in' port is just used for simulation, i.e., it is not needed in our design. The 'reg_in' port is the output of this module and acts as an input to the other logic in FPGA. The BEEcube Platform Studio provides the MATLAB API

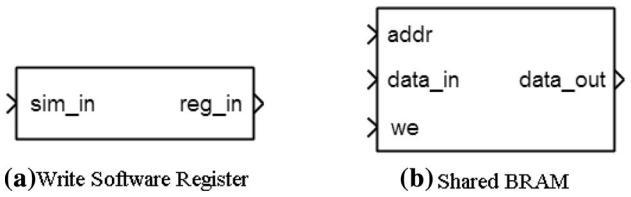

Fig. 4 Two methods for data interchange

function 'bee4_reg_write' associated with the 'write software register.' A defined 32-bit data value appears at the 'reg_in' port after using this function to write a data to the module.

Another way for data interchange is 'Shared BRAM' or 'Shared Block RAM.' It can be used to access medium-sized blocks of data in both hardware and software. This module creates a dual-port Block RAM on the FPGA, which is shared between software and hardware. The ports of 'Shared BRAM' are shown in Fig. 4b. 'addr' is the address to be loaded from the Block RAM on the next cycle. The bit width of this port can be defined by user. 'data_in' is the data port where other logic in FPGA can write data into the 'Shared BRAM.' 'we' is a control port and when asserted 'we' high, the current value of 'data_in' will be written to the address present on 'addr.' The 'data_out' port will output the data contents in 'Shared BRAM' loaded from the previous address and it is not needed in our design. After other logic writes the data to 'Shared BRAM' module, 'bee4_bram_read' function can be used in MATLAB to obtain the data stored in it.

4 Beam experiments

4.1 Bunch-by-bunch position acquisition

The bunch-by-bunch beam position acquisition system was tested on the storage ring at SSRF, with expected results of beam experiments. Figure 5 shows the ADC raw data when SSRF was in operation at user time.

Equation (2) is used to obtain the bunch-by-bunch position. Figure 6 shows the horizontal and vertical position of bunch 43 (bunch 43 is the first bunch with charge), 83, 123 and 163 in 20 turns. The waveform of each bunch position is expected the same as Libera TBT position data. The horizontal amplitude of each bunch does not differ significantly, while the vertical amplitude becomes greater for the bunches at rearward position.

4.2 System resolution

To estimate the system resolution under different signal amplitudes, we used the bunch charge distribution in

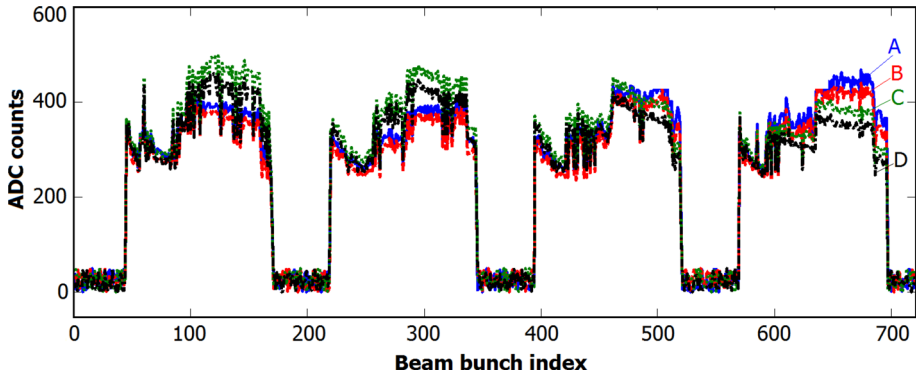

Fig. 5 ADC raw data of Channel *A*, *B*, *C* and *D* (bunch No. 43 is the first bunch with charge)

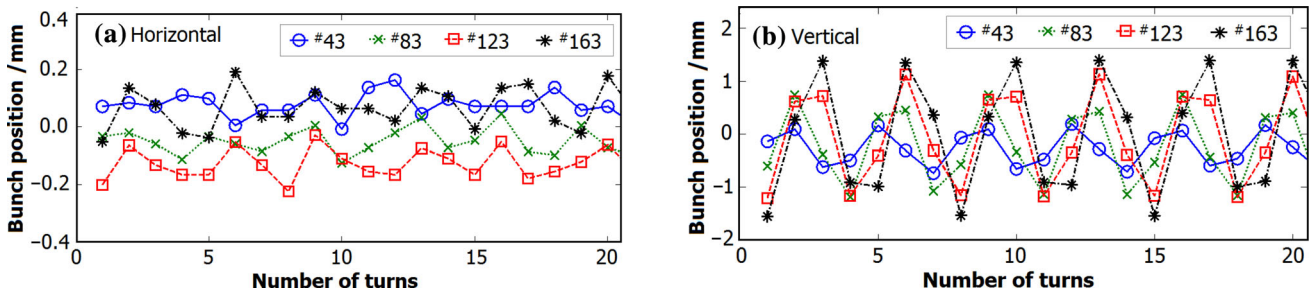

Fig. 6 Bunch-by-bunch positions in 20 turns

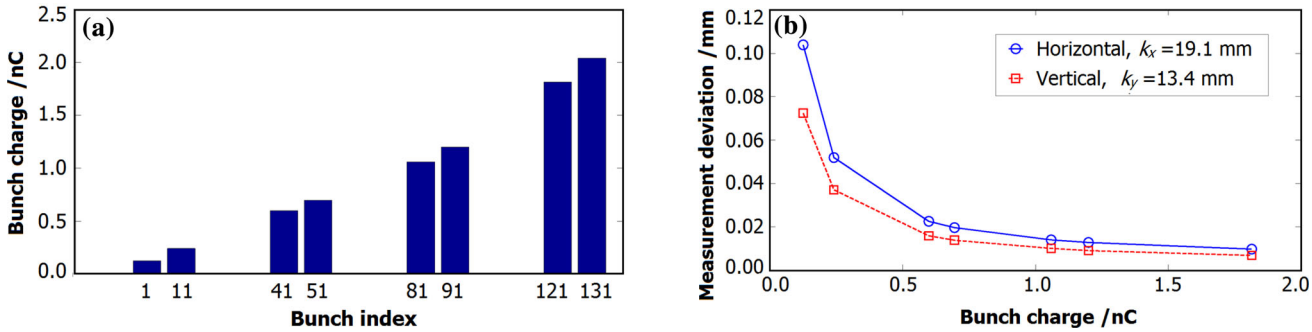

Fig. 7 Bunch charge distribution to estimate system resolution (**a**) and the system resolution under different bunch charges (**b**)

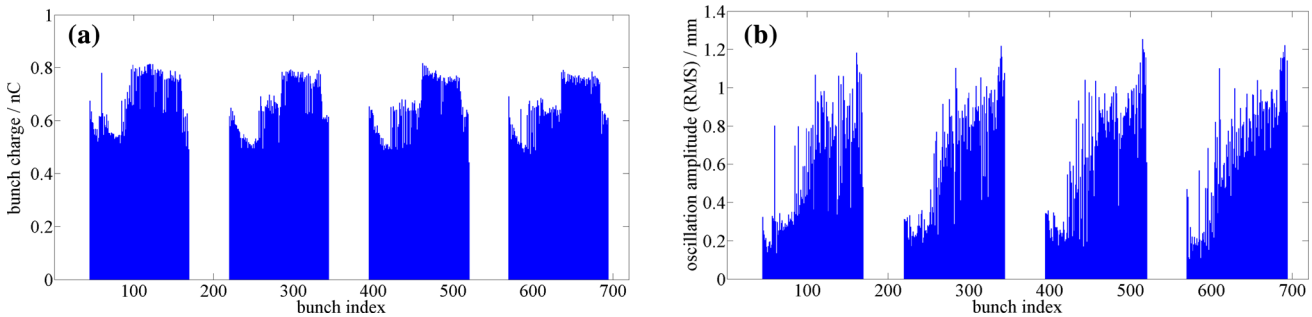

Fig. 8 Bunch charge distribution (**a**) and oscillation amplitude when beam scraper is open (**b**)

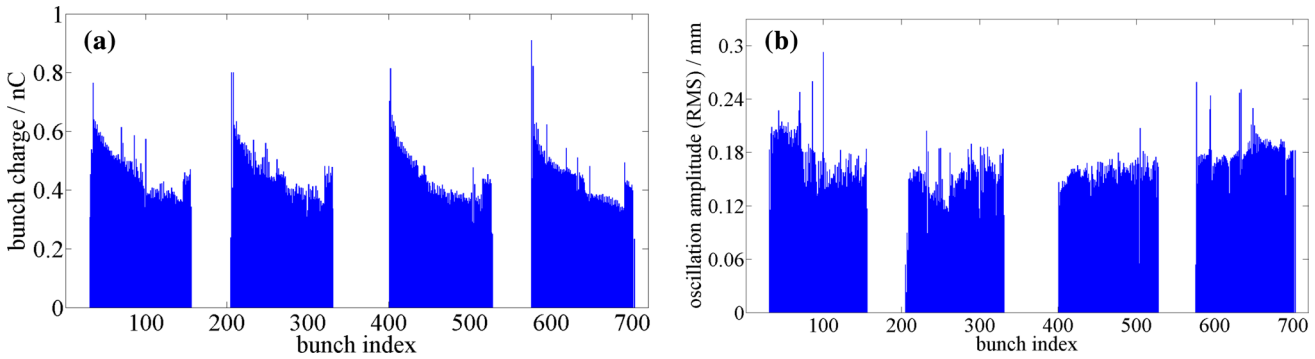

Fig. 9 Bunch charge distribution (**a**) and oscillation amplitude when beam scraper is closed (**b**)

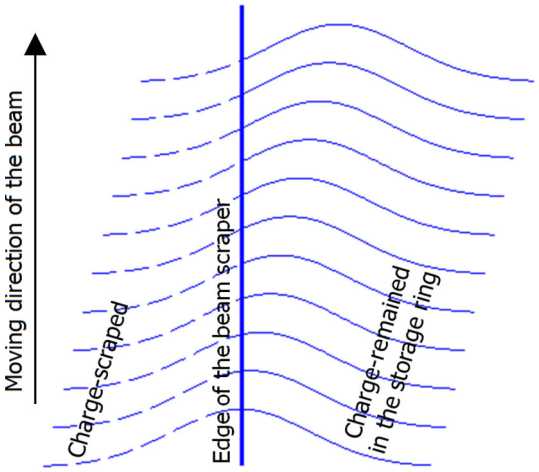

Fig. 10 Phenomenon when a bunch train passes through the beam scraper

Fig. 7a and calculated the RMS value of the position in 2000 turns, as shown in Fig. 7b. It can be seen that for signal of strong enough intensities, the system resolution can be better than 10 μm.

4.3 Multi-bunch instability

When the storage ring is in multi-bunch mode, bunch interaction occurs. The bunch at rearward position is excited by the wakefield of front bunch, and its amplitude of transverse oscillation becomes greater. Figure 8 shows bunch charge distribution and oscillation amplitude when the beam scraper is open. If we close the scraper, bunch charge will be scraped as shown in Fig. 9. More charge is scraped for the rearward bunch since its oscillation amplitude is greater when the scraper is open. After scraping, oscillation amplitude is limited by the scraper and the bunch amplitude does not differ significantly from each other.

Figure 10 shows the above phenomenon when a bunch train passes through the beam scraper. The amplitude of transverse oscillation is greater for the bunch at rearward position, and more charge is scraped.

5 Conclusion

A bunch-by-bunch beam position acquisition system at SSRF has been developed. The wideband synthesizer and high-performance FPGA hardware DAQ platform are used in the system. The FPGA logic and relevant software have been implemented. The BPM raw data and the bunch-by-bunch position have been measured, and the system resolution is better than 10 μm and beam instability of multi-bunch can be observed.

To improve the accuracy of position measurement, as the task of our further research, we will utilize wideband amplifiers to amplify the origin beam signal to close to the full scale of ADC, or use automatic gain control to eliminate the beam current effect.

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