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# Modeling operation amplifier based on VHDL-AMS for TID effect

**Jin-hui Liu[1] · Quan Wang[1] · Ying Zhang[1] · Gang Liu[1] · Bo Wan[1]**

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**Abstract** A model of the operational amplifier based on VHDL-AMS is proposed. According to needs of simulating the total ionizing dose (TID) radiation effect, parameters of operational amplifier are taken into account when the performance is specified. The operational amplifier model used for the TID radiation effect simulation is completed after verifying each modeled parameter. And a parameter for describing the external environment is introduced to make the model combined with TID. Finally, an example is used to illustrate the TID effect on the operational amplifier of MC14573, proving the validity of the model.

**Keywords** Behavioral modeling · Operational amplifier · Total ionizing dose (TID) · Radiation effects · VHDL-AMS

## 1 Introduction

It is well known that the space radiation environment consists of a variety of energetic particles and environments of high-level ionizing radiations create special challenges in designing integrated circuit [1]. When a radiation particle strikes a semiconductor material, it may generate total ionizing dose (TID) effect and single event effect (SEE) [2, 3]. SEE is a bit flip in a memory element or transient voltage pulse occurred in the combinational logic [4, 5]. Cumulative damage of the semiconductor lattice may be caused by TID, leading to the shift in threshold voltage, an increase of leakage current, etc. [6]. Radiation dose can be expressed in rad, i.e. the absorption of 100 erg per gram of matter, often specified as silicon (Si) or $SiO_2$. Studies have been done to investigate radiation effects on semiconductor devices and characterize performance of electrical components. As a common component, operational amplifier (op-amp) is modeled to investigate the TID effect [7].

Although the model of op-amp can be built up by SPICE-like methods (Simulation Program with Integrated Circuit Emphasis), the memory and computing time required by SPICE grow very fast with the size of integrated circuit [8]. The behavioral modeling technique takes less time to reach the acceptable accuracy limits [9]. VHDL-AMS [10] is a derivative of VHDL (VHSIC Hardware Description Language, VHSIC—Very High Speed Integrated Circuit) to define the behavior of analog and mixed-signal systems (AMS). A series of experiments have shown that the behavioral model based on VHDL-AMS is better than SPICE model in validity and accuracy.

A model for TID effect based on VHDL-AMS allows a system design to be simulated with TID awareness before manufactured, so as to facilitate quick comparisons of alternatives and to test correctness of the design without hardware prototyping [11–14].

In this paper, we present a configurable op-amp model based on VHDL-AMS for TID effect application. The basic architecture and characteristics of an op-amp are introduced. The op-amp model with the interface representing TID is verified by comparing the results of computer simulation and experimental measurements.

✉ Quan Wang
qwang@xidian.edu.cn

[1] Research Institute of Computer Peripherals, Xidian University, Xi'an, Shaanxi Province, China

## 2 Operational amplifier

Operational amplifier is an essential device in the IC. When an appropriate feedback network is provided, it can work as precision AC or DC amplifier, active filter, oscillator, voltage comparator, etc. [15]. Generally, performance of an op-amp can be characterized by its input, middle, and output parts [16].

### 2.1 Basic model

Each part of the basic op-amp model has its function [17, 18]. The input part provides appropriate quiescent current for each part of op-amp by comparing the inverting and non-inverting input terminals. The gain is generated by a high resistance in the middle part, which converts the quiescent current to a large voltage. The output part provides an output drive, in essence, a current gain, via the output impedance. Figure 1 shows the model of the basic op-amp.

In the basic model, Node 1 is the inverting input terminal, Node 2 is the non-inverting input terminal, Node 81 is output of the op-amp, Nodes 101 and 102 are, respectively, the positive and negative power supply (which are always symmetrical), and Node 100 is the reference voltage relative to the voltage of Node 103.

### 2.2 Characteristics of basic model

The ideal op-amp can be summarized as follows: the output attempts to make the voltage difference between the inputs zero, and no current flows into the inputs. It also has infinite input impedance, infinite pass bandwidth, zero output impedance, infinite gain, etc. Obviously, the real op-amp cannot provide such ideal characteristics.

In the middle part, $G_1$, $R_{P1}$, and $C_{P1}$ can characterize the op-amp gains. The open-loop gain of the op-amp $A_{vol}$ is calculated by Eq. (1),

$$A_{vol} = K_{G1} \cdot R_{P1}, \tag{1}$$

where $K_{G1}$ is the gain of the current source controlled by the voltage difference between Nodes 5 and 6. The first-pole frequency $f_{p1}$ provides the classic low-pass filter response of the op-amp. It can be modeled by a simple RC filter with its frequency being determined by Eq. (2).

$$f_{p1} = 1/(2\pi \cdot R_{P1} \cdot C_{P1}). \tag{2}$$

The unit-gain frequency $f_u$, or the gain–bandwidth product, is a constant specified by the manufactures. The frequency of input AC signal should be less than $f_u$.

$$f_u = A_{vol} f_{p1} \tag{3}$$

The voltage change rate is described by Slew, which is limited by the maximum transistor current $I_{G1}$,

$$\text{Slew} = I_{G1}/C_{P1}. \tag{4}$$

$I_{G1}$, the current of source $G_1$, can be determined by Eq. (5)

$$I_{G1} = K_{G1}[V(5) - V(6)]. \tag{5}$$

If $R_{G1} = R_{G2}$, the voltage difference is

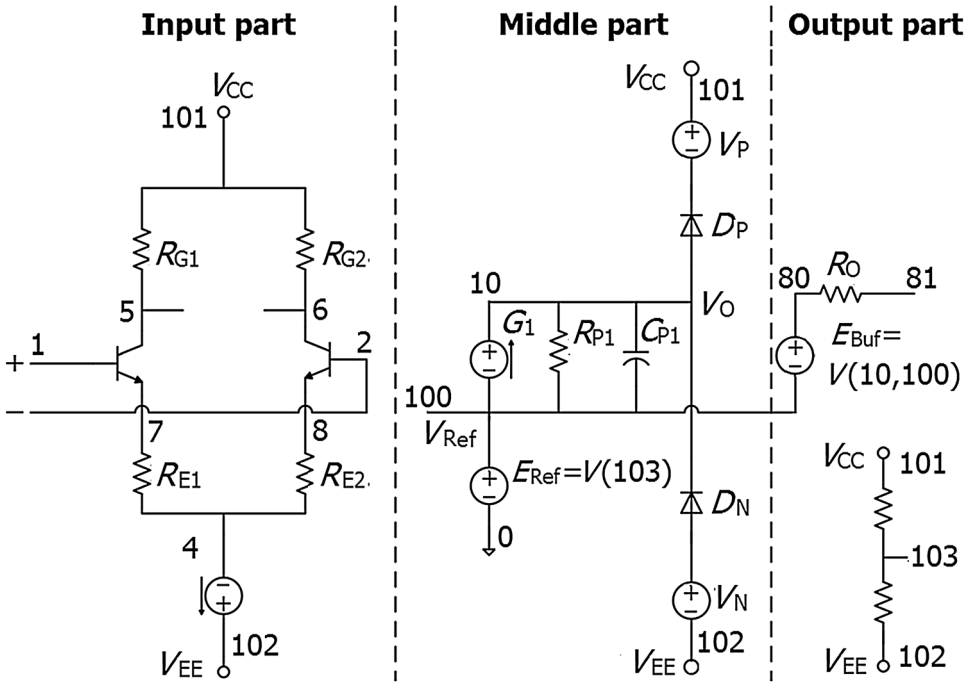


**Fig. 1** The basic model

$$V(5) - V(6) = R_{G1}(I_{C1} - I_{C2}), \quad (6)$$

where $I_{C1}$ and $I_{C2}$ are collector currents of the transistors. $I_{G1}$ becomes

$$I_{G1} = K_{G1}R_{G1}(I_{C1} - I_{C2}). \quad (7)$$

Choose $R_{G1} = 1/K_{G1}$, the current is

$$I_{G1} = I_{C1} - I_{C2}. \quad (8)$$

The middle part contains all the gains and describes the output voltage limit $V_{limit}$, a guarantee that the output voltage is less than the power supply. The difference between the output and supply voltages is less than $V_{limit}$.

$$(V_{CC} - V_{out}) < V_{limit} \quad (9)$$

Hanging a diode and a voltage source from the supply rails is a common way to limit or clamp a maximum voltage swing of the circuit. Current source $G_1$ and resistor $R_{P1}$ develop a voltage signal that swings positive until diode $D_P$ begins to conduct through $V_P$ clamping the output voltage.

$$V_{out\_max} = V_{CC} - V_{limit} \quad (10)$$

$V_{limit}$ is determined by the on-voltage of diode, $V_d$, and the source voltage, $V_P$

$$V_{limit} = V_P - V_d. \quad (11)$$

The model for the output stage is a simple voltage-controlled voltage source (VCVS), whose output is described by $V_{EBUF} = K_{EBUF}\cdot[V(10) - V(100)]$, where $K_{EBUF} = 1$. $R_O$ is output resistance of the op-amp.

In addition to the characteristics explained above, it is necessary for the op-amp model to elaborate some other characteristics for the TID effect simulation, including input bias current ($I_B$), input offset voltage ($V_{OS}$), common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR).

## 3 Advanced model

The parameters mentioned above can be modeled by appending some devices to optimize the op-amp model. The parameter models shall be verified by corresponding test circuits through the SystemVision, which provides a development environment to design and verify designs consisting of digital, analog, and mixed-signal electronics. In each test circuit, the op-amp parameters can be configured and obtained by computer simulations. By comparing the simulation results to the set values, the accuracy can be proved.

### 3.1 Modeling bias current and testing

Although, ideally, no current flows into input terminals of an op-amp, in practice there are always two input bias currents. The bias current is the average of the two input bias current. The bias current provides a quiescent current required by the transistor to ensure that the input stage can be driven properly. As a result, the bias current makes a voltage produced in the output. In order to simulate the bias current, a current source $I_{BOFF}$ is added between the inputs to drive the transistor device in Fig. 2.

The bias current $I_B$ is

$$I_B = (I_{B1} + I_{B2})/2, \quad (12)$$

where $I_{B1}$ and $I_{B2}$ are the currents flowing into non-inverting terminal and inverting terminal, respectively.

The circuit to test bias current is shown in Fig. 3. $I_{B1}$ and $I_{B2}$ can be obtained as follows:

1. Measure the output voltage $V_{O1}$ by switching on $S_1$ and $S_2$, and measure the output voltage $V_{O2}$ by keeping $S_2$ on and switching off $S_1$. On the basis of KVL, we have:

$$I_{B1} = (V_{O1} - V_{O2})/R_1. \quad (13)$$

2. Measure $V_{O3}$ by switching on $S_1$ on and switching off $S_2$, we have:

$$I_{B2} = (V_{O3} - V_{O1})/R_2. \quad (14)$$

In the circuit in Fig. 3, set $R_1 = R_2 = 1\ M\Omega$ and make the input impedance of the millivoltmeter large enough to reduce the load impact, simulations can be done with different values of $I_B$ obtained by measuring $V_{O1}$, $V_{O2}$, and $V_{O3}$. The simulation results are shown in Table 1.

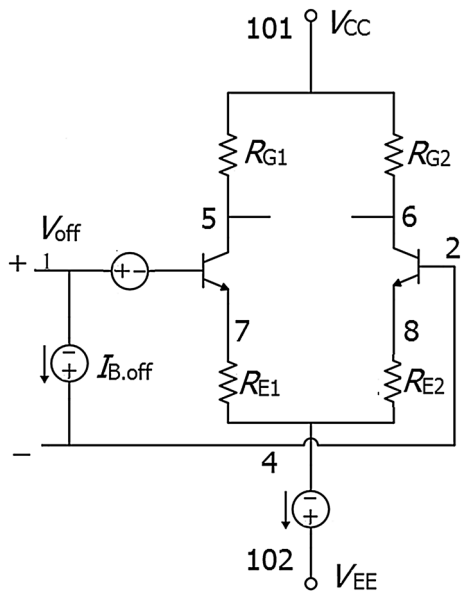


**Fig. 2** The input offset voltage and the bias current model

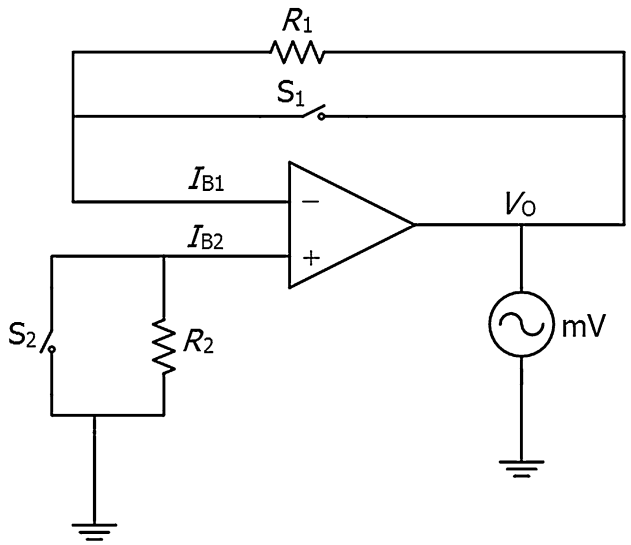


**Fig. 3** The test circuit for $I_B$

### 3.2 Modeling input offset voltage and testing

Related to mismatches in input bias currents, the input offset voltage is required across the op-amp input terminals to drive the output voltage to zero. Ideal amplifier produces 0 V out for 0 V inputs which means no input offset voltage, namely the differential inputs are totally symmetrical. However, due to imperfections in the differential amplifier that constitutes the input stage, the input offset voltage exists in op-amp. With the model in Fig. 2, let the op-amp output be zero by adjusting the input offset voltage in the condition of zero inputs, a DC voltage source $V_{OFF}$ can be accessed to the input stage to model the input offset voltage.

The input offset voltage and the bias current model can be verified by a test circuit. It is worth noting that the error produced by the test circuit should be less than the offset voltage, when the input offset voltage is a few micro volts. The standard circuit for testing the input offset voltage is shown in Fig. 4, where the input offset voltage is amplified with the gain 1001 and the output of the op-amp is measured by the precision digital voltmeter. Through the output voltage and the op-amp gain, the offset voltage ($V_{OS}$) can be derived.

$$V_{OS} = V_{out}/1001 \tag{15}$$

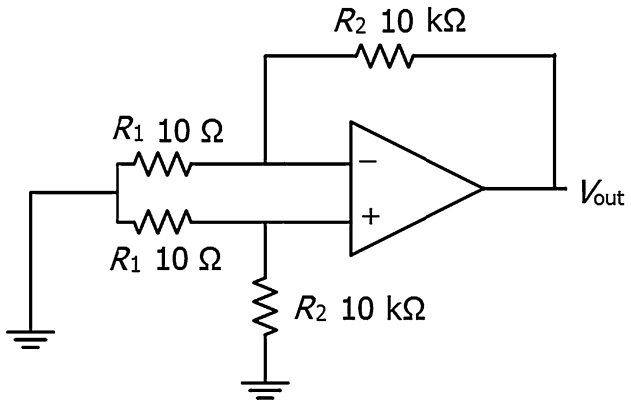


**Fig. 4** The test circuit for $V_{OS}$

Using the VHDL-AMS model, simulation results obtained with different offset voltages are shown in Table 2, and the relative error of $V_{OS}$ is about 0.9 %.

### 3.3 Modeling CMRR and testing

A perfect op-amp amplifier only has a voltage difference between its two inputs, completely rejecting any voltages that are common to both. Due to mismatching in the transistors and resistors of the input stage, the common-mode voltage produces a small differential error voltage at the input terminals. This error can be amplified right along with any other input signal. A standard measure to this defect is called the CMRR, which can be considered as the ratio of differential signal gain to the common-mode signal gain expressed in dB:

$$\begin{aligned} \text{CMRR} &= A_v/A_{CM} = [V_{out}/(v_+ - v_-)] \cdot [V_{CM}/V_{out}] \\ &= V_{CM}/(v_+ - v_-), \end{aligned} \tag{16}$$

$$v_+ - v_- = V_{CM}/\text{CMRR}, \tag{17}$$

where $A_v$ is the different gain and $A_{CM}$ is the common-mode gain, and $V_{CM} = v_+ = v_-$ is the differential error voltage produced at the input. The circuit model CMRR of an op-amp is shown in Fig. 5.

According to Fig. 5, we have the following equations:

$$V_{CM} = V(105) - V(100), \tag{18}$$

$$\begin{aligned} V(30,100) &= [V(105) - V(100)]/\text{CMRR} \\ &= [V(105) - V(100)] \cdot K_{GCM} \cdot R_{CM}. \end{aligned} \tag{19}$$

**Table 1** Simulation results of bias current

| Groups | Set value (nA) | $I_{B1}$ (nA) | $I_{B2}$ (nA) | Relative error of $I_{B1}$ (%) | Relative error of $I_{B2}$ (%) |
|---|---|---|---|---|---|
| 1 | 60.00 | 59.51 | 59.48 | 0.82 | 0.87 |
| 2 | 150.00 | 149.51 | 149.48 | 0.33 | 0.35 |
| 3 | 250.00 | 249.50 | 249.48 | 0.20 | 0.21 |
| 4 | 340.00 | 339.50 | 339.48 | 0.15 | 0.15 |

**Table 2** Simulation results of offset voltage

| Groups | Set value (mV) | Measured value (mV) | Relative error (%) |
|---|---|---|---|
| 1 | 0.900 | 0.892 | 0.89 |
| 2 | 1.00 | 0.991 | 0.90 |
| 3 | 1.20 | 1.189 | 0.92 |
| 4 | 1.50 | 1.487 | 0.87 |

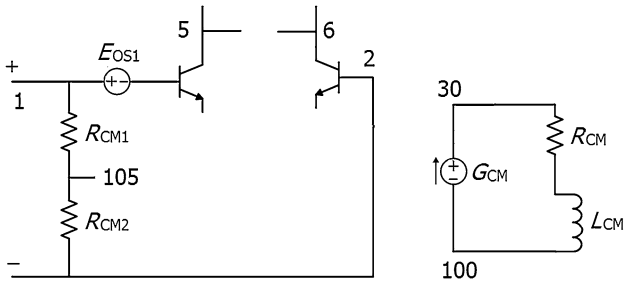


**Fig. 5** The CMRR model

Based on $V_{CM}$, $G_{CM}$ is a current source controlled by the voltage of node 105 with the gain of $K_{GCM}$. Then, the common-mode error voltage is the voltage $V(30,100)$. The error voltage should be added to the output by placing EOS at the positive input terminal, that is a voltage source controlled by $V(30,100)$ at gain = 1.

The CMRR can be measured by the circuit in Fig. 6. It has four precision resistors to configure the op-amp as a differential amplifier. For $R_1 = R_2 = 1$ kΩ, at input voltages $V_{in1}$ and $V_{in2}$, and the corresponding output voltages of $V_{out1}$ and $V_{out2}$, we shall have Eq. (20) for CMRR:

$$\text{CMRR} = [\Delta V_{in}/\Delta V_{out}](1 + R_2/R_1), \tag{20}$$

where, $\Delta V_{in} = V_{in1} - V_{in2}$, and $\Delta V_{out} = V_{out1} - V_{out2}$. Setting different values of CMRR and measuring the test circuit, the simulation results in Table 3 can be obtained.

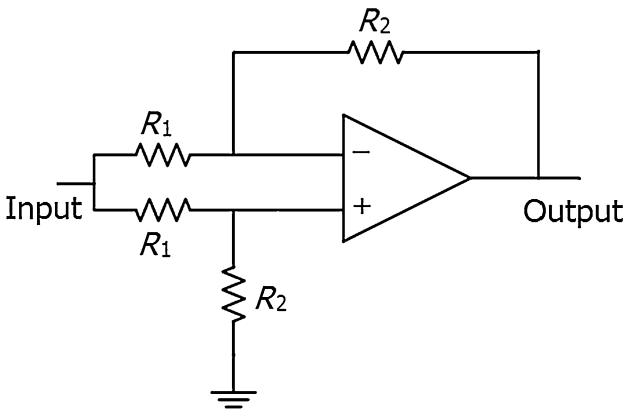


**Fig. 6** The test circuit for CMRR

**Table 3** Simulation results of CMRR

| Groups | Set value (dB) | Measure value (dB) | Relative error (%) |
|---|---|---|---|
| 1 | 108.00 | 113.80 | 5.37 |
| 2 | 101.00 | 106.92 | 5.86 |
| 3 | 89.00 | 94.99 | 6.73 |
| 4 | 85.00 | 91.00 | 7.06 |

### 3.4 Modeling PSRR and testing

An ideal op-amp should have infinite power supply rejection ratio, i.e. the noise of power supply has no effect on the output. PSRR is defined as the ratio of the change in supply voltage in the op-amp to the equivalent output voltage it produces, a term that qualifies the ability of a circuit to reject the noise from the power supply. The model of PSRR is shown in Fig. 7.

Where EPSY is a voltage-controlled voltage source with the coefficient $K_e$. The voltage of the controlled source is $V(30,100) = K_e \cdot V(V_{CC},V_{EE})$. The PSRR can be represented as:

$$\text{PSRR} = K_e R_1/R_2. \tag{21}$$

Then, insert a voltage source $E_{OS2}$ controlled by the voltage of node 22 at the input stage to indicate the influence of the power supply. The model of PSRR can be verified by the test circuit [19]. In Fig. 8, DUT is the op-amp to be measured while $A_1$ works as buffer amplifier.

Provide the supply voltages of $V_{S1}$ and $V_{S2}$ are different from each other, and so are the corresponding output voltages of $V_{out1}$ and $V_{out2}$, we shall have

$$\Delta V_s = V_{s1} - V_{s2}\,\text{PSRR} = 101\Delta V_S/\Delta V_{out}, \tag{22}$$

where, $\Delta V_S = V_{S1} - V_{S2}$, and $\Delta V_{out} = V_{out1} - V_{out2}$. The simulation results are given in Table 4.

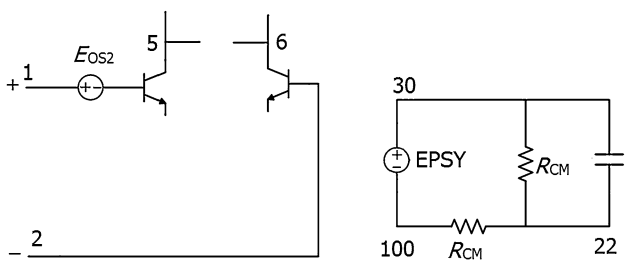


**Fig. 7** The PSRR model

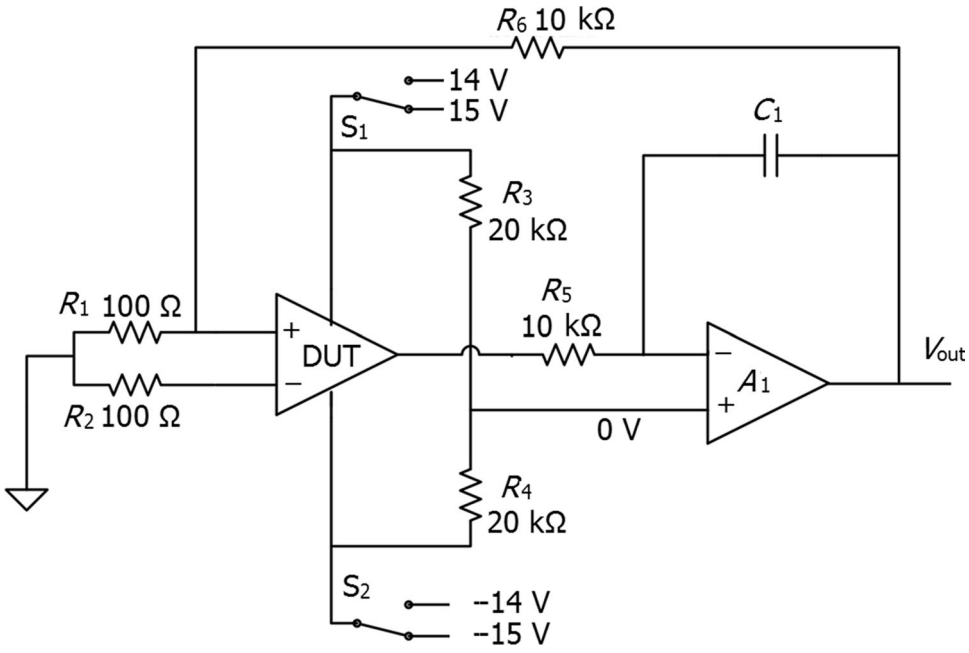


**Fig. 8** The test circuit for PSRR

### 3.5 Modeling the TID effect

As mentioned in Sect. 1, this op-amp model is used for the TID effect simulation so that the parameter Dose is introduced to describe the environmental factor [20]. The TID effect increases with the irradiation dose, hence the device failure. Performance of the op-amp can be described by a relationship between the parameter *Dose* and any other parameter of the op-amp:

$$P_{\mathrm{TID}} = f(\mathrm{Dose}, p) \tag{23}$$

where $p$ can be any parameter of $I_{\mathrm{B}}$, CMRR, PSRR, etc., and $P_{\mathrm{TID}}$ is the corresponding parameter affected by TID. In practice, every type of op-amp has its own performance parameter $p$, through radiation, $p$ becomes $P_{\mathrm{TID}}$. The function $f$ can be extracted from a large number of experimental data by the mathematical method.

Now, the op-amp model is a configurable model composed by the basic op-amp model and the parameter models. From the parameter test results, it can be seen that the simulation results conform to the set value. The relative errors of $I_{\mathrm{B}}$ and $V_{\mathrm{OS}}$ are less than 1 %, while the relative errors of CMRR and PSRR are about 10 %. Because of the negative feedback network, the set value of CMRR is sometimes difficult to achieve. In practice, CMRR, as a reference value in the IC manufacturing process, can range up and down about 10 %. The parameter Dose reflects the TID effect on op-amp under ionizing irradiation.

**Table 4** Simulation result of PSRR

| Groups | Set value (dB) | Measured value (dB) | Relative error (%) |
|---|---|---|---|
| 1 | 95.00 | 88.98 | 6.33 |
| 2 | 88.50 | 82.48 | 6.80 |
| 3 | 84.00 | 77.98 | 7.17 |
| 4 | 80.00 | 73.98 | 7.52 |

## 4 Comprehensive test simulation

Every modeled parameter has been verified to show its feasibility, but this is insufficient to show correctness of the op-amp model. Therefore, more experiments in particular about the external factor effect on op-amp are needed. A series of experiments were done to study the TID effect on the op-amp and verify the model to describe the effect.

In order to simulate the TID effect, first, the characteristics were obtained by the experiments of different irradiation doses. Next, according to the characteristics at certain irradiation doses, a curve was drawn to describe the variation of characteristic. Finally, choose a certain radiation dose to verify the model by comparing the results of simulation and experiment. The curve is introduced by the parameter $P_{\mathrm{TID}}$ in op-amp model.

Figure 9a shows an op-amp physical circuit for TID effect experiments, with the circuit shown in Fig. 9b. There are four operational amplifiers integrated in the circuit. The op-amp is of the MC14573 type. The output signals are $V_{\mathrm{out1}}$ to $V_{\mathrm{out4}}$ with the +5 V/−5 V power supplies and excitation source. From Fig. 9b, we have:

$$V_{\mathrm{out}} = 5.5\,V_{\mathrm{in}}. \tag{24}$$

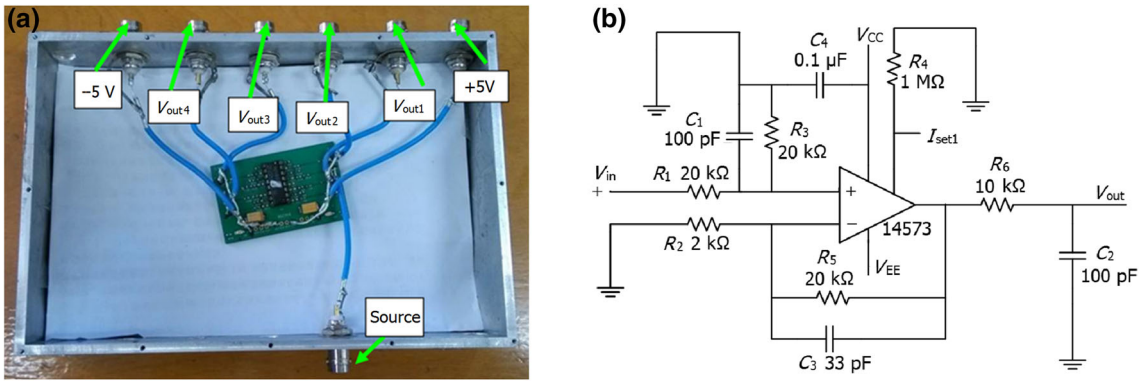


**Fig. 9** The experiment set-up (**a**) and circuit of the op-amp circuit, (**b**) the schematic diagram of the set-up

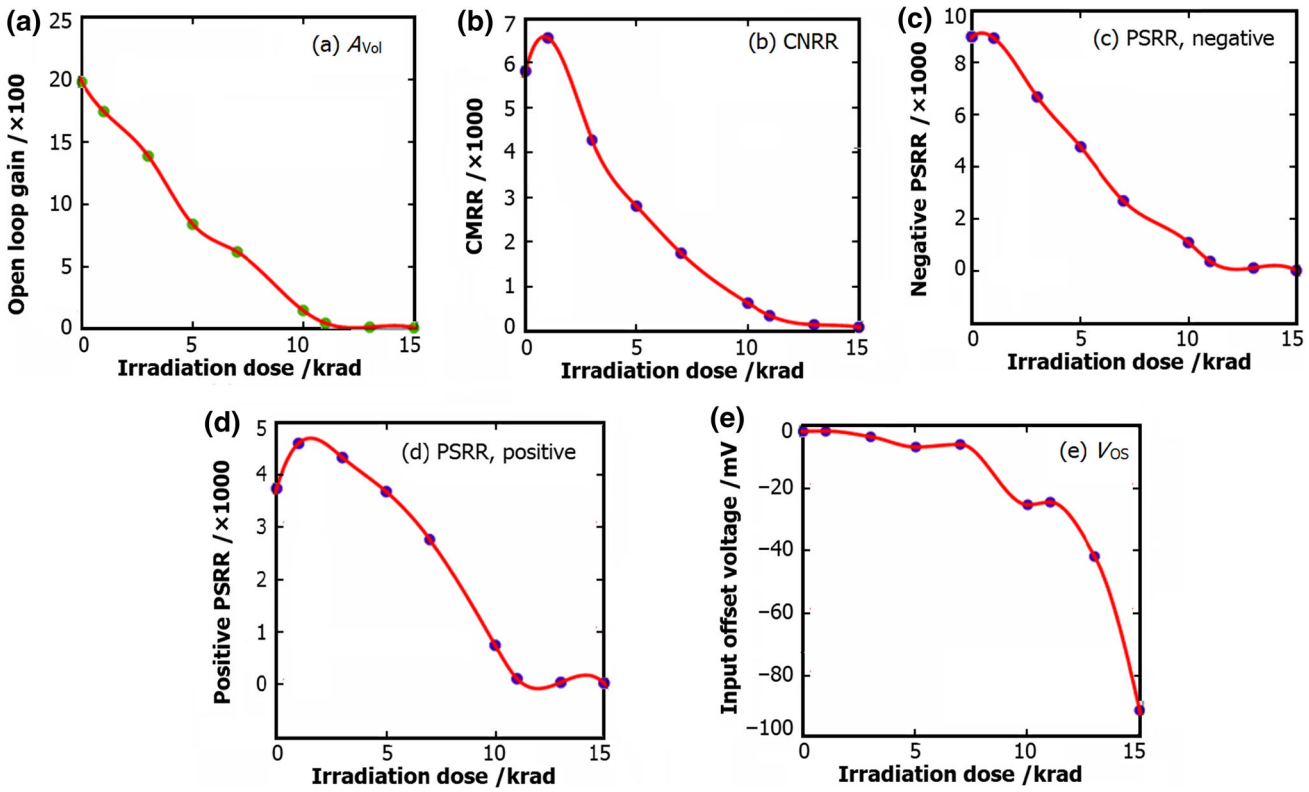


**Fig. 10** Parameters of the MC14573 irradiated to different TIDs

The setup was irradiated in a $^{60}$Co gamma-ray source at the dose rate of 10 rad/s. As shown in Fig. 10, the characteristic varied with the irradiation dose. The data were calculated from the measurements, and the curves were obtained by the method of cubic spine interpolation. The parameters of MC14573 changed significantly when the irradiation dose is greater than 5 krad, probably causing failure of the device. A shift in threshold might be caused by TID; hence, the changes in the input offset voltage and the open-loop gain. The leak current may result in changes in the PSRR.

Choose a certain dose on the curves, and parameters of the op-amp can be obtained for verifying the models. The doses of 0, 1, and 3 krad at 10 mV sine input were chosen, because when the input is a few mV changes, the output is easier to be observed. The outputs and simulation results at 0, 1, and 3 krad are shown in Fig. 11a–c, respectively. The simulated peak-to-peak voltage is about 105 mV, while the actual circuit is about 110 mV. It can be seen that the TID increase causes a shift of output, but the component still works properly.

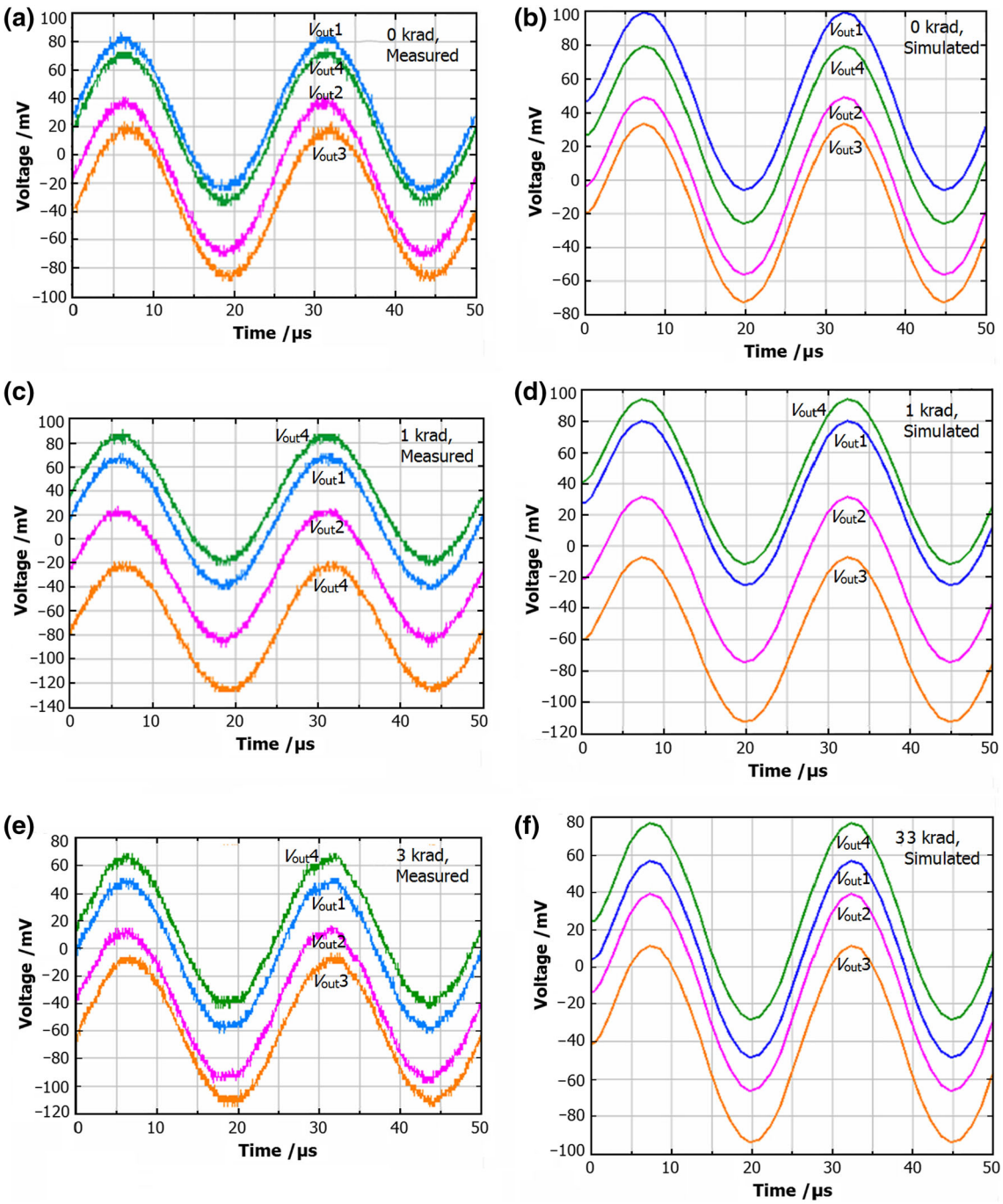


**Fig. 11** Experiment and simulation results at 0–3 krad, with 10 mV sine input

## 5 Conclusion

An op-amp model is established based on VHDL-AMS and validated by a series of experiments. According to the internal topology, a basic model of op-amp is built up. The behavior models of performance parameters are set up to make the op-amp model more complete. By changing the generic parameters of the model, op-amps of different performances can be used to simulate the TID effect. An interface is introduced to make the model associated with the external environment representing TID effect on the performance of op-amp. A series of experiments were performed to test the TID effect, and corresponding schematic was built up and simulated. The simulation results proved that the op-amp model is effective and accurate, and the TID effect research methodology is feasible.

The intention of this model is to be general, so the future work is to design a series of proper experiments to verify

that the model can be used to simulate different kinds of op-amps.

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