Reduction of self-heating effect in SOI MOSFET by forming a new buried layer structure

ZHU Ming, LIN Qing, LIU Xiang-Hua, LIN Zi-Xin, ZHANG Zheng-Xuan, LIN Cheng-Lu

(State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, the Chinese Academy of Sciences, Shanghai 200050)

Abstract An inherent self-heating effect of the silicon-on-insulator (SOI) devices limits their application at high current levels. In this paper a novel solution to reduce the self-heating effect is proposed, based on N^+ and O^+ co-implantation into silicon wafer to form a new buried layer structure. This new structure was simulated using Medici program, and the temperature distribution and output characteristics were compared with those of the conventional SOI counterparts. As expected, a reduction of self-heating effect in the novel SOI device was observed.

Keywords SOI, Self-heating effect, Co-implantation, Medici simulation

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1 Introduction

The silicon-on-insulator (SOI) technology exhibits many advantages over bulk silicon technology such as the reduction of parasitic capacitances, excellent subthreshold slope, elimination of latch up and resistance of radiation,[1] so that it is widely used in the realm of high-speed, high-temperature and low-power circuits. In a SOI MOSFET there is a buried oxide layer, typically between 100~400 nm thick, to achieve desired electrical isolation. But this layer is also a barrier to heat flow from the channel, because the thermal conductivity of SiO_2 is approximately 100 times less than that of silicon.[2] Inevitably, temperature of the channel will increase while the device is operating, thus the self-heating effect becomes an inherent issue of SOI MOSFET. A rise of more than 100℃ in channel temperature has been reported for devices with typical VLSI dimensions and operating conditions.[3] As device geometries shrink, and transconductance and current density increase with MOS scaling, the self-heating effect becomes more pronounced. In the past decade, several attempts have been made to reduce the temperature raise due to self-heating effects in SOI devices, including reduction of the buried oxide thickness, quasi-SOI technology,[4] etc., but these solutions will introduce other disadvantages in the meantime.

In this paper, we propose a new SOI structure to reduce the self-heating effect. The buried layer of this SOI structure is formed by N^+ and O^+ co-implantation into silicon wafer, and it is a sandwich layer that consists of silicon dioxide (upper part), silicon oxynitride (medium part) and silicon nitride (lower part). Because of the much smaller thermal conductivity of silicon oxynitride and silicon nitride than that of silicon dioxide, the heat produced in the channel when the device operates is easily dissipated. Thereby the influence of self-heating effect can be reduced in our novel SOI device.

First of all, the fabrication of this new structure will be introduced in the paper. The microstructure was then examined by cross-sectional transmission electron microscopy (XTEM). Moreover, numerical simulations were carried out with a two-dimensional device simulation program Medici (TMA, 2000) to predict the electrical characteristics and thermal behavior.

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2 Experimental

Different from the conventional SIMOX (separation by implanted oxygen) technology where O^+ implantation is carried out to form the buried oxide layer, in our experiment the insulator layer is formed by N^+ and O^+ co-implantation into the Si (100) substrate. The details are as fellows. At first the N^+ implantation was performed with a $9.0\times10^{17}cm^{-2}$ dose at 150keV. The samples were subsequently annealed for 2 h at 1200℃ in flowing N_2 gas. Then O^+ was implanted with a fluence of $3.5\times10^{17}cm^{-2}$ at 110keV, keeping temperature of the target during implantation being approximately 550℃. At last the as-implanted samples were annealed for 5 h at 1250℃ in a gas mixture of Ar and O_2.

Fig.1 shows an XTEM photograph of the annealed samples. An excellent SOI structure is formed and the interfaces of top Si/buried layer and buried layer/substrate are very abrupt. And we also find the buried layer is a sandwich structure consisting of silicon dioxide (upper part), silicon oxynitride (medium part) and silicon nitride (lower part). From the photo we have calculated the thickness of every part of buried layer, they are 50 nm, 101 nm and 79 nm respectively.

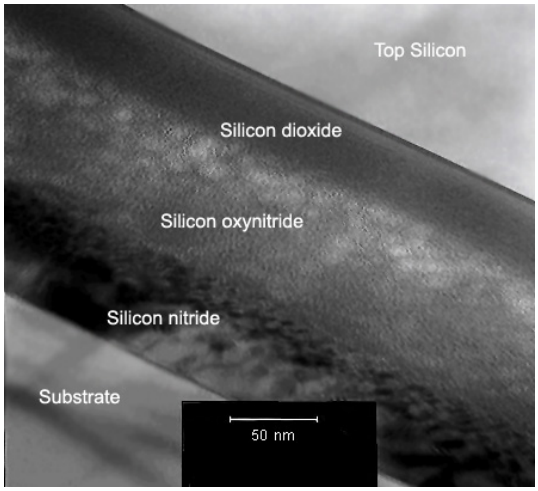

Fig.1 A cross-sectional XTEM micrograph of the buried sandwich layer structure by N^+ and O^+ co-implantation.

3 Device design and simulation

The novel SOI MOSFET (Fig.2) was fabricated on the new structure SOI wafers mentioned above. The most relevant geometrical and technological parameters are as follows. The device consisted of a p-type substrate doped with a density of $1\times10^{16}cm^{-3}$ and n-type source and drain doping of $2\times10^{17}cm^{-3}$. The gate oxide thickness was 20 nm. According to Fig.1, thicknesses of top silicon, silicon dioxide, silicon oxynitride and silicon nitride were 173 nm, 50 nm, 101 nm and 79 nm, respectively. Medici program was used to examine the self-heating effect and the device temperature distribution. To make a comparison with the novel structure, we designed a conventional SOI MOSFET, which parameters were the same as the former, but the buried layer was only silicon dioxide of 230 nm thick that equaled the total thickness of the three buried layers in the novel structure.

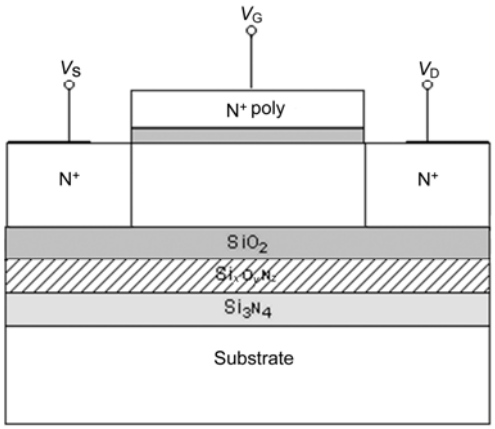

Fig.2 Cross-sectional schematic of the proposed novel SOI MOSFET structure with buried sandwich layer.

Fig.3 shows the temperature 3D distribution of the conventional SOI device. Axes *X* and *Y* represent the horizontal and vertical dimensions of the device, respectively. Temperature in the substrate due to the self-heating effect was only 300 K while the channel temperature increased to 570 K. The temperature distribution of the new structure design is shown in Fig.4. It is observed that the channel temperature for the new device simulation was about 480 K, significantly lower than 570 K for the conventional SOI device simulation. The simulated output characteristics of the two different devices with and without self-heating effect were compared in Fig.5. In the simulations we made the gate voltage equal to 10 V because a higher V_{GS} led to a more obvious self-heating effect.

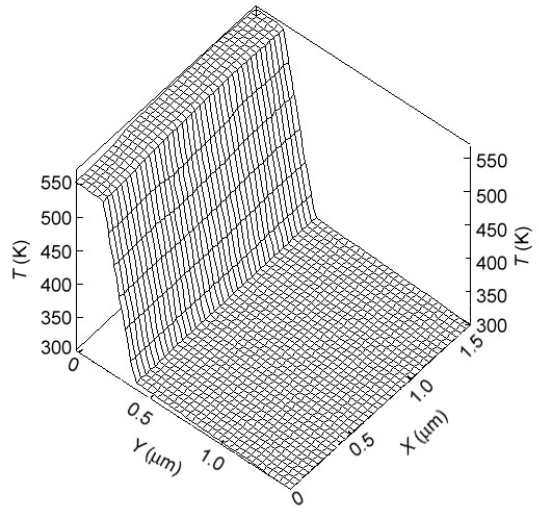

Fig.3 Temperature 3D distribution of a conventional SOI device by Medici simulation.

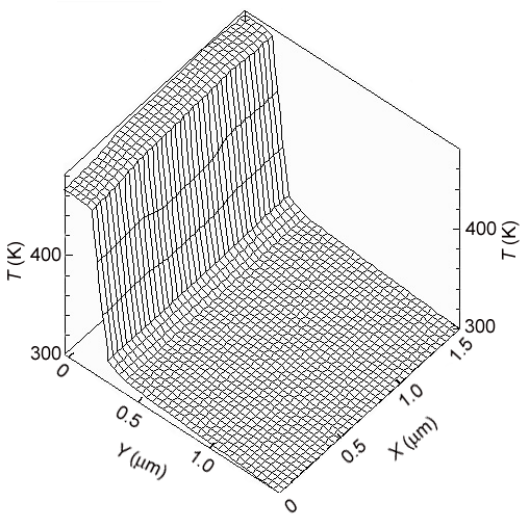

Fig.4 Temperature 3D distribution of the novel SOI device by Medici simulation.

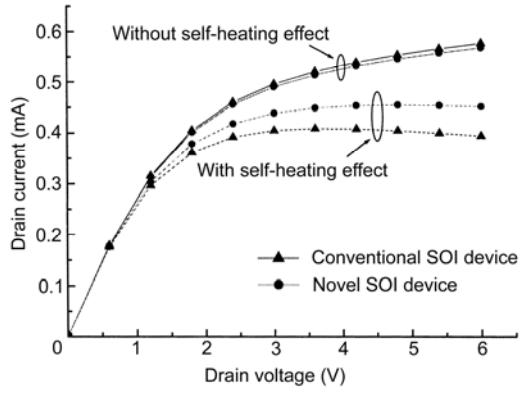

Fig.5 Simulated I_{DS}-V_{DS} characteristics of conventional and novel SOI MOSFET.

4 Results and discussions

In the output characteristic curves a negative differential resistance (NDR) is observed when self-heating effect is considered, which can be explained as that a significant increase of temperature occurs in the channel because of the relatively poor thermal conductivity of the buried layer. It is understood that the mobility is sensitive to the temperature and it decreases as the temperature rises. And the drain current will decrease due to the degradation of the mobility. Thus the NDR emerges on the output characteristics. We know that the more serious the influence of self-heating effect, the more obvious the NDR will be, thereby we can examine self-heating effect by the I_{DS}-V_{DS} curves.

From Fig.5 we know that, in the bias conditions of V_{GS} = 10 V and V_{DS} = 6.0 V, there is a decrease of 31.7% for the drain current in the conventional SOI device if the self-heating effect is considered. As compared with that, there is only a decrease of 20.5% in the new SOI device with a sandwich buried layer. So the resultant curves demonstrate that, as expected, influence of the self-heating effect is weakened when the novel structure is used. From Fig.3 and Fig.4 we can draw the same conclusion because the channel temperature of new SOI device is much lower than that of the conventional one.

McDaid[5] reported a formula about the difference between the channel and ambient temperature ΔT_c

$$\Delta T_c = \frac{P_t \cdot t_b}{K_b A} \tag{1}$$

where t_b is the thickness of the buried layer, K_b is the thermal conductivity of the buried layer and A is the area over which the power is generated (taken as the effective channel length multiplied by the device width). Because the thermal conductivity of silicon nitride or silicon oxynitride is much smaller than that of silicon dioxide, and in our simulations thickness of the buried silicon dioxide layer is much smaller in the new structure than that in the conventional one, according to Eq.(1), ΔT_c of the novel SOI device is much lower, in other words the heat spreads into the silicon substrate through the insulator layer in the case

of new structure.

5 Conclusions

For reducing the self-heating effect in SOI devices, a novel technique has been proposed. We use N^+ and O^+ co-implantation to form a buried sandwich layer, which combines silicon dioxide, silicon oxynitride and silicon nitride. This new structure has been simulated using Medici. Device temperature distributions and output characteristics are examined. The simulative results show that the channel temperature was reduced and the NDR was weakened. It demonstrated that the self-heating effect was reduced.

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