Fabrication of thick BOX SOI by Smart-cut technology

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Abstract A SOI material with thick BOX (2.2 μm) was successfully fabricated using the Smart-cut technology. The thick BOX SOI microstructures were investigated by high resolution cross-sectional transmission electron microscopy (XTEM), while the electrical properties were studied by the spreading resistance profile (SRP). Experimental results demonstrate that both structural and electrical properties of the SOI structure are very good.

Keywords SOI, Thick BOX, Smart-cut

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1 Introduction

Silicon-on-insulator (SOI) materials, with which a silicon dioxide insulating layer between the top Si layer and the substrate permits considerable improvements in the performance of microelectronic circuits produced by very large scale integration (VLSI) and is a promising technology in the rapidly growing field of microelectromechanical systems (MEMS), are now being used with a wide range of Si-SOI and buried oxide thickness.[1] While the SOI materials for fully-depleted CMOS devices have top Si and BOX (buried oxide) of 10~100 nm and 50~200 nm, respectively, the applications for "thick BOX SOI", including high-voltage switching, MEMS and sensors, need a BOX layer of more than 400 nm. In the application of high-voltage SOI devices, the breakdown voltage (BV) is decided by the lateral breakdown voltage and the vertical breakdown voltage, and design of the former is similar to that of the bulk silicon devices,[2] but the latter, BV(vertical), is limited by the thickness of Si layer (T_{Si}) and that of buried oxide layer (T_{ox}). An approximate expression[3] was given as

$$\mathrm{BV(vertical)} \approx E_c(\frac{1}{2}T_{Si} + 3T_{ox})$$

where E_c represents electric field applied between the drain and the substrate. In order to gain high breakdown voltage, a thick BOX SOI substrate is required.

At present, SIMOX (Separation by Implanted Oxygen) and Smart-cut technology have become the mainstream SOI technologies. In SIMOX technology, the silicon dioxide layer is formed by oxygen implantation through the top surface of a standard bulk wafer. Thicker layers require higher doses, and the resulting damage in the top silicon increases with the dose.[4,5] Moreover, two key processes (oxygen implantation and annealing) in SIMOX fabrication are very expensive.[6-8] Since the thickness limitation of SIMOX for the implanted oxide layers is 0.4 μm, another choice for thick BOX SOI substrate fabrication must be made. In this work, we fabricate the SOI substrate with a BOX thickness of about 2.2 μm by the Smart-cut technology. The Smart-cut process is very strict on the surface microroughness, usually less than 1 nm, a target very difficult to attain for the thick oxided Si wafer bonding. With an increase of the buried oxide thickness, the probability of total deformation of the bonded SOI wafers is also increased.[9] We successfully fabricated the thick BOX SOI by strictly controlling oxidation process and bonding technique. And their excellent microstructure and electrical properties were proved by the XTEM (cross-sectional transmission electron microscopy) and SRP (spreading resistance profile).

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2 Experimental

The experimental conditions in this study are as follows.

(1) A thermal oxide layer of 2.2 μm was grown on the support wafer A. The oxidation process was carefully performed to ensure a good surface microroughness. This oxide layer would become the future thick buried oxide.

(2) 6×10^{16} cm^{-2} hydrogen ions were implanted into 3-inch Si wafer B at energy of 150 keV. The Si layer above the H^+ projected range would be transferred to the support wafer and become the device layer of the SOI wafer.

(3) Wafer A and wafer B were hydrophilic bonded at room temperature. Both wafers were previously cleaned using a modified RCA process. This step also plays a key role in this process.

(4) It was reported that interface energy of room temperature bonded hydrophilic Si/SiO_2 wafers obviously changes with time during storage in air at room temperature to 150℃.[10] In order to achieve a high interface energy of bonded wafers, the bonded pairs were maintained at low temperature (150℃) for about 30 h in this study. Then a two-step heat treatment of the two bonded wafers was performed. During the first step (500℃), implanted wafer B split into two parts: the top Si layer of the SOI structure and the remainder of wafer B. After the splitting had occurred, high-temperature annealing was performed at 1100℃ for 1 h to improve the bonding strength and reduce defect, and the final SOI structures were obtained.

Fig.1 shows the schematic steps of the process. The as-obtained SOI structure was investigated by XTEM and SRP.

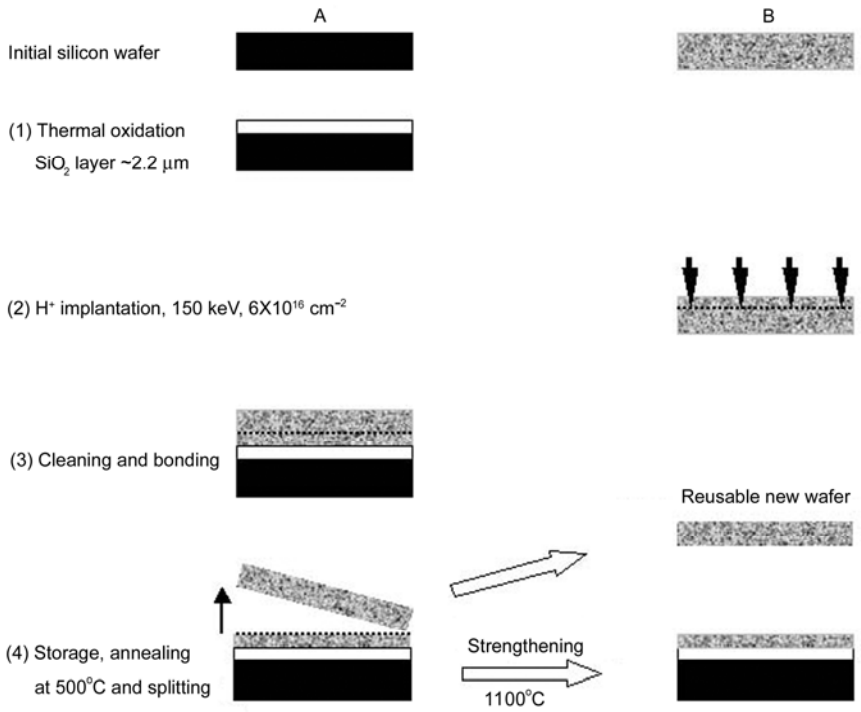


Fig.1 Schematic of the smart-cut process.

3 Results and discussions

Cross-sectional TEM was adopted to investigate the microstructure of SOI. The image of the as-formed SOI structure is shown in Fig.2. It gives a direct evidence of the formation of SOI structure. The thickness of the top Si is about 1.1 μm, similar to the value of calculated H^+ projected range from the computer program TRIM-96. The thickness of buried oxide layer is about 2.2 μm, measured from the graph and in agreement with the expectant result.

The high resolution XTEM micrographs of these wafers at the top Si/BOX interface and BOX/Si interface are shown in Fig.3. These interfaces are very ab-

rupt and the interface between the crystal Si and the amorphous BOX is easily discerned in both cases. Both top silicon and substrate Si have an excellent single crystal quality with no resolvable defects. The undulation of the Si-SiO_2 bonded interface between top Si and BOX is only about 2 or 3 lattices (as shown in Fig.3(a)), and the interface between the BOX and Si substrate has comparatively small undulation as well (as shown in Fig.3(b)).

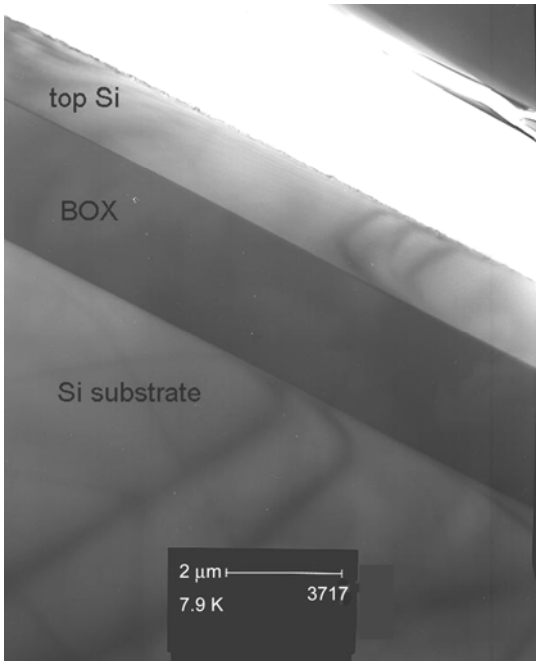
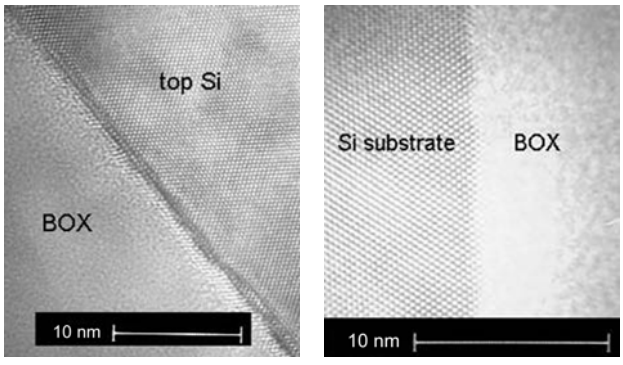


Fig.2 An XTEM micrograph of the Smart-cut SOI structure.



(a) (b)

Fig.3 High resolution XTEM micrographs of (a) the top Si/BOX interface and (b) the BOX/Si substrate interface in a thick BOX SOI wafer.

The spreading resistance profile was employed to study electrical properties and thickness of the layers. The result is shown in Fig.4. The spreading resistance of the top Si is only about $(1\sim2)\times10^4$ Ω. It increases to more than 10^8 Ω (exceeding the measurement range of the SRP apparatus) rapidly at a depth of 1.1 μm (corresponding to top Si/SiO_2 interface). At a depth of more than 3.3 μm (corresponding to SiO_2/Si substrate interface) the spreading resistance sharply drops to 8×10^4 Ω. All the results indicate the existence of sharp interfaces of the top Si/SiO_2 and SiO_2/Si. And the deeper BOX interface is a little shaper than the upper BOX interface. This is in good agreement with the results of XTEM. The high resistive layer at the depth from around 1.1 μm to around 3.3 μm has a spreading resistance of higher than 10^8 Ω, suggesting excellent dielectric properties of the SiO_2 layer with a thickness of about 2.2 μm. The spreading resistance of the top Si is not very homogeneous, which can be attributed to some residual stress in silicon film. The effects of different top Si thickness on the spreading resistance will be studied in future.

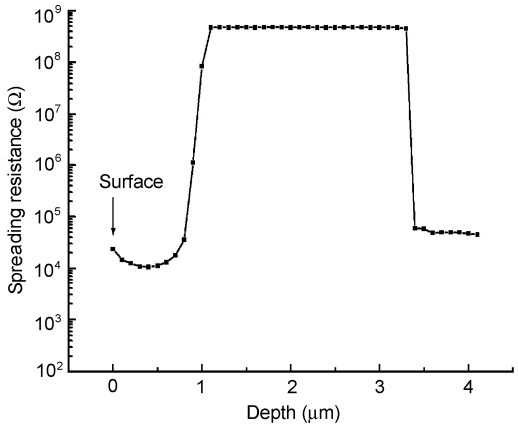


Fig.4 Spreading resistance profile of the SOI substrate.

4 Conclusions

In conclusion, thick BOX SOI materials, which are important in applications such as power devices, MEMS, etc, have been successfully fabricated by the Smart-cut process. The XTEM micrograph confirms the formation of the SOI structure. In addition, high resolution XTEM images have verified good qualities of both top Si and silicon/insulator interfaces. And SRP results demonstrate excellent electrical properties of our SOI materials. The sample is proved to be suitable for high voltage device and other applications.

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