Transient radiation effects in CMOS inverters fabricated on SIMOX and BESOI wafers*

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Abstract CMOS inverter circuits are successfully fabricated on thin film SIMOX wafers and thick film BESOI wafers. The output voltage variation is measured with a pulse of γ-ray radiation. Compared with bulk silicon CMOS circuits, SOI circuits have improved the transient radiation hardness significantly.
Keywords Transient radiation effects, SIMOX, BESOI, CMOS

1 Introduction

In recent years, SOI (silicon on insulator) technology has been developed rapidly and is regarded as a primary candidate for the 21 st century ICs (integrated circuits). One of the most important advantages is that SOI circuits are inherently tolerant to transient irradiation and single event upsets.[1] Many SOI fabrication techniques have been investigated. Among those, SIMOX (separation by implanted oxygen) and BESOI (bonding and etch-back SOI) are the most potential techniques.[2,3] High quality thin film SIMOX wafers have been fabricated by the multi-implant-and annealing technique. BESOI wafers have high quality Si overlayer and buried oxide, but the etch-back is a difficult process. It is suitable to fabricate thick film SOI wafer. In this paper, CMOS (complementary metal-oxide-semiconductor) inverter circuits have been successfully fabricated on the thin film SIMOX wafers and the thick film BESOI wafers. The transient radiation response for the inverters is investigated by measuring output voltage variation with a pulse of γ-ray radiation.

2 Experimental

(100) oriented, 10~13Ω·cm, P-type, single crystal silicon wafers were implanted by 200 keV O^+ at a dose of $0.6\times10^{18}cm^{-2}$ and annealed at 1300°C for 2 h in the 0.99 volume fraction Ar+0.01 volume fraction O_2 ambient. After three times implanting and annealing, the Si overlayer thickness and the buried oxide thickness of the final SIMOX wafer are 180 nm and 430 nm, respectively. A standard process (silicon gate, self-alignment, total ion implantation) was used to fabricate the linear gate cc4069 CMOS circuits (six inverters). The silicon island was formed by high temperature oxidation of isolating groove with Si_3N_4 mask. The gate oxide was grown by dry O_2 oxidation and the thickness is 58 nm. The channel width/length ratio is 128 μm/2.5μm and 344 μm/2.5μm for PMOS and NMOS, respectively. The final thickness in the active region is approximately 135 nm, so both PMOS and NMOS are fully-depleted.

In dry oxygen ambient at 1100°C, 300 nm SiO_2 was grown onto (100) oriented, 3~6Ω·cm, N-type, single crystal silicon wafers. After suitable surface treatment they were bonded directly in $H_2 + O_2$ ambient at 1200°C for 2 h. One side of the bonded wafers was thinned down to approximately 6 μm by mechanical polishing. The cc4007 CMOS circuits (double complementary pairs and an inverter) were fabricated on the BESOI wafers. P well was pushed into the buried oxide directly. The gate oxide was grown to 98 nm in O_2, H_2+O_2, O_2 ambients

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at 1000°C sequentially. The channel length is 7.5 μm.

The γ-dot experiments were performed at the Chinese Academy of Engineering Physics. The dose rate was 6.56×10^8 Gy(Si)/s. The bias condition during irrradiation is $V_{DD} = 5V$, $V_{ss} = 0V$, the input terminal (1A) of one of the inverters connects to earth, and the corresponding output terminal (1Q) connects with an oscillograph. The residual input terminals connect to earth and the residual output terminals are floating.

3 Results and discussion

The output voltage variation of the inverters on thin film SIMOX, thick film BESOI and bulk silicon with a pulse of γ-ray radiation is shown in Fig.1(a), (b) and (c), respectively. For SOI devices, there are approximately 4μs output disturbance after 6.56×10^8 Gy(Si)/s γ-ray radiation, and the amplitude of SIMOX devices is smaller than that of BESOI devices. For comparison, the output voltage of bulk devices suffers 2 μs level turnover, followed by 3.8μs level rise after 5.97×10^8 Gy(Si)/s γ-ray radiation. The transient radiation hardness of SOI devices is significantly better than that of bulk devices. Furthermore, thin film totally-depleted SOI devices are harder to transient radiation than thick film partly-depleted SOI devices.

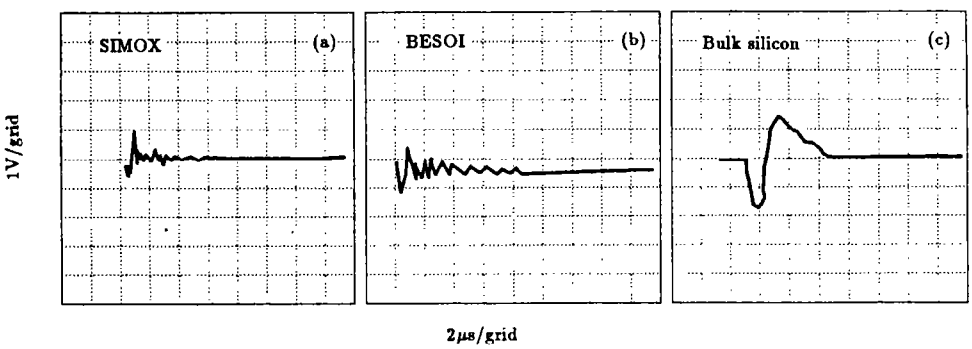

Fig.1 The output voltage variation of the inverters on (a) thin film SIMOX, (b) thick film BESOI and (c) bulk silicon with a pulse of γ-ray radiation

It is well known that the prompt transient photocurrent, I_{PDS}, induced by a pulse of γ-ray radiation, causes the output voltage variation.[4] While,

$$I_{PDS} = q \cdot V_{depl} \cdot g \cdot \dot{D}(t)$$

where $\dot{D}$(t) is the dose rate, g is the electron-hole generation rate ($4\times10^{15}\,cm^{-3}\cdot Gy^{-1}$(Si)), q is the elementary charge, V_{depl} is the depletion volume. SOI devices have smaller V_{depl} and eliminate the latch-up effect due to the buried oxide, so the transient radiation hardness is better than that of bulk devices.

4 Conclusion

CMOS circuits have been successfully fabricated on the thin film SIMOX wafers and the thick film BESOI wafers. The transient radiation effects are studied by measuring the output voltage variation with a pulse of γ-ray radiation. Compared with bulk circuits, SOI circuits have excellent hardness to transient radiation.

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