A VMEbus interface for multi-detector trigger and control system

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Abstract MUSE (MUltiplicity SElector) is the trigger and control system of CHIMERA, a 4π charged particles detector. Initialization of MUSE can be performed via VMEbus. This paper describes the design of VMEbus interface and functional module in MUSE, and briefs an application of MUSE.

Keywords VME (Versa Module Europa), Bus, Interface, Trigger

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1 INTRODUCTION

CHIMERA is a 4π charged particles detector for intermediate energy nuclear reaction studies and is manufactured by INFN-LNS (Istituto Nazionale di Fisica Nucleare-Laboratori Nazionali Del Sud) in Italy.[1] MUSE (MUltiplicity SElector) is a trigger and readout control system to generate various delay gate signals to start/stop QDC and TDC module. There are about 5000 electronic channels in the CHIMERA, and the rate of event expected is around 1 kHz. The QDC and TDC (mod VN1465 and VN1488) are two types of VME9U module manufactured by CAEN. They will form a daisy chain to acquire data from Multi-detector system and to transfer data to CPU or disk-recorder in block transfer mode under the MUSE controlling. The MUSE can accept instructions from the Master (i.e. FIC8234) or VME crate controller to initiate. The VMEbus interface design in MUSE is accordance with the protocol VME64 REV. D1.6.[2]

The VMEbus is defined an interfacing system used to interconnect data processing, storage, control device and peripheral. The block diagram of VME bus is shown in Fig.1. The VMEbus have itself mechanical structure and functional structure that include three parts: VMEbus signal lines (four groups of bus), backplane interface logic and functional module. The backplane provide Data Transfer Bus (DTB), Priority Interrupt Bus, Arbitration Bus and Utility Bus. The functional modules are such as Master, Slave and Location monitor etc. The DTB is a standard parallel data transfer bus, it's an

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asynchronous, and has all together 34 types of cycles that can be divided into Read cycle, Write cycle, Block read cycle, Block write cycle and multiplexed cycle.

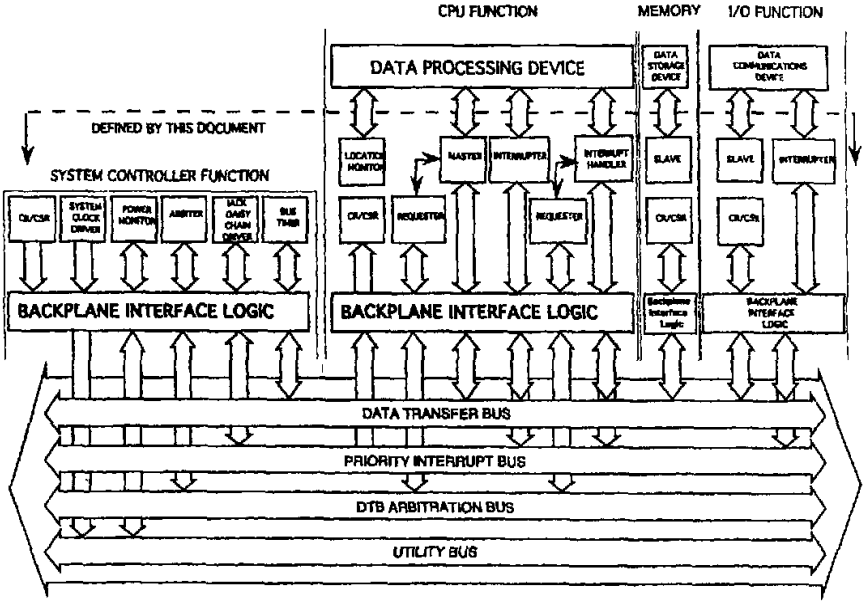

Fig.1 The functional block diagram of VMEbus

2 THE LAYOUT OF THE VMEbus INTERFACE IN MUSE

The block diagram of VMEbus interface in MUSE is shown in Fig.2. The address bus and data bus of the MUSE are all 32 bits, the higher base address bits (A31-A24) will be used to preset module's address. Two rotary switches are used here, and one ($20FFE000) is for CBLT operation, another ($32xxxxxx) is for normal read/write operation. Only Address Modify code 0B and 09 can be accepted, so AM code logic module just produces a strobe signal (AC3) to partake reading and writing. Two data strobe signals DS0 and DS1 are also to do reading and writing, and don't be used to access address thanks to the MUSE do not employ byte-access. The MUSE produces two pairs of differential signals Long-Word-write (WE/-WE) and Long-Word-read (R/-R) to write and to read, don't use signal WE of the VME directly to write if WE is low level and to read if WE is high. In order to simplify design of this interface circuit, the MUSE is always set up first board in daisy chain during physics experiment.

In the MUSE, pattern memory, FDL (Fast Data Link) memory and normal registers can be accessed via VME bus. Two memories are composed of CMOS static RAM

TC551402J (TOSHIBA high speed static random access memory, max. access time 25 ns), working at × 1 bit mode and 22 address lines. So the address lines of the VMEbus are not enough to assign for above three parts, the MUSE use a special address register and translator (i.e. LS138) to strobe them, any one of them may not be accessed before accessing this special register.

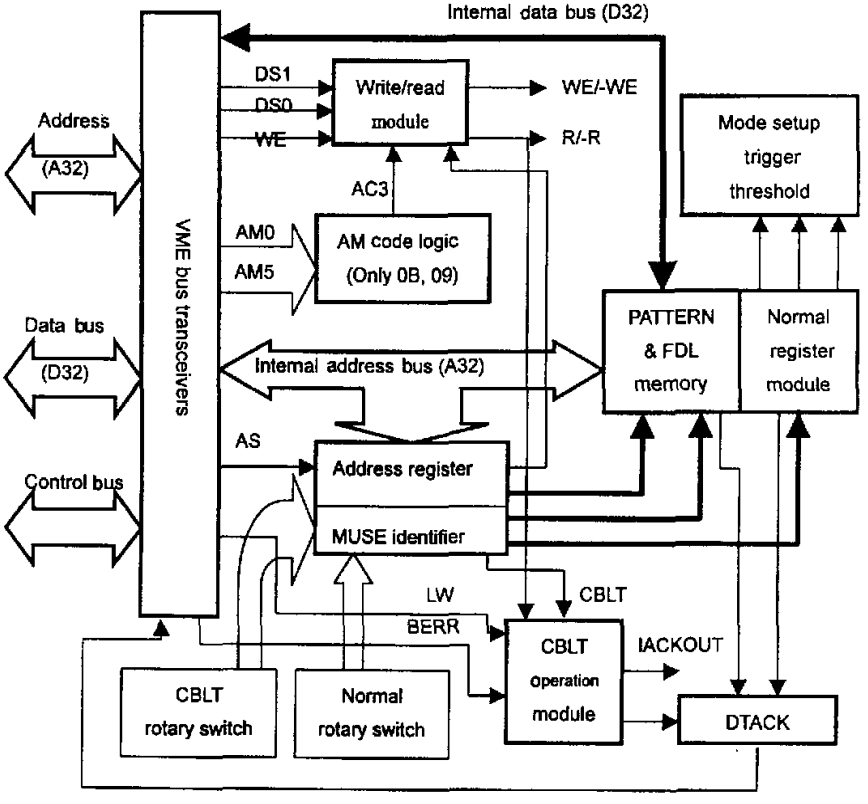

Fig.2 The block diagram of VME interface in MUSE

The MUSE must control data to transfer in CBLT operation as soon as the QDC and TDC data buffer are full. When each CBLT operation was happening, the MUSE was asked to transfer three data as heads, the data are good event counts, online pattern location and End-of-Block-Register. In CBLT mode, the MUSE enable IACKOUT immediately after completing above three data transfer and disable it when the last board makes a BERR signal.

There are not other interrupter bus signals except IACKIN/IACKOUT in the MUSE, and arbitration bus signal don't employ anyone. The address bus and data bus I/O cir-

cuit of the MUSE are made of bi-directional transceivers IDT74FCT16543 that has high speed low-power and high drive outputs, and control signal I/O chip is also to select products of IDT Company — IDT74FCT16245.

3 INITIALIZATION OF THE MUSE

To initialize the MUSE, the pattern memory and FDL memory must be accessed via VME bus. Even internal data bus has 32 lines, but the pattern memory data bit is just one (D0) and FDL memory are four data bits (D3–D0). We need to fill full all pattern memory and FDL memory with our desired value. In addition, we need to setup working mode-Multi-event input or single event input, trigger mode — Internal or External trigger, manual or remote mode, ADC-GATE delay time and width of eight channels, threshold of each discriminator in 13 channels and etc.

4 TESTING PROGRAMS FOR MUSE TRIGGER CIRCUIT

In order to test circuit design of the MUSE, we wrote various programs to check each function module via VMEbus. The main testing programs are listed in below Table.

Table 1 Testing programs for MUSE

File name	Functions
GFDL.C	Write datum into FDL memory a assigned address
GRFDL.C	Read out datum from FDL memory a assigned address
GTPATT.C	Write 0x0 into all location of pattern memory
G2.C	Write 0x1 into a assigned address of pattern memory, 0x0 to others
G1.C	Write 0x1 to pre-trigger memory a assigned address, 0x0 to others
GWCHA.C	Write delay time and gate width into GD-memory
GLTCW.C	Write COINC Wind. Delay time (9500-CW) into GD-memory
GLTPCW.C	Write PRECOINC Wind. Delay time (9500-PCW) into GD-memory
G3B.C	Include G1.C, GLTCW.C, GLTPCW.C, GFDL.C, G2.C (for single event mode)
GTBTA.C	Read operation for event counter FIFO, online PATTERN FIFO, and End-of-Block-Register
GTBLT.C	CBLT operation for event counter FIFO, online PATTERN FIFO, and End-of-Block-Register
G7.C	Select a MPX channel to output, load different threshold for 13 discriminator which are used to generate an event pattern
GACQ.C	Output Enable/Disable "ACQ." signal
GMUSE.C	Write INT/EXT trigger mode and work mode register
RESET.C	Output a "RESET" signal
GFE.C	Include RESET.C, GMUSE.C, GACQ.C, G7.C
GRFE.C	Read out all mode settings for MUSE

5 EXPERIMENT RESULT

The MUSE were successfully used in REVERSE physics experiment in October 1999. The MUSE acted a trigger circuit of the CHIMERA for 4-Pi charged particles detector. And the trigger is based on the analysis of a combination of multiplicity and logic signals (up to 10) coming from the CHIMERA array and/or from any other coupled device. These signals can be combined to generate an event pattern compared with the predefined valid patterns in order to accept or reject the event. If the event is accepted (good event), the MUSE opens the gates of associate QDC and TDC to convert data. If the event is rejected (bad event), the gates are closed, a clear signal is sent to all QDC and TDC modules. The MUSE worked in the single event mode, and to delivery a FDL strobe at the end edge of each ADC-BUSY signal, then, to wait END-CPU signal from CPU (FIC8234) to remove dead time, and ready to accept a new event.

References

1 INFN-LNS: Activity Report, 1996-1999
2 VME64 draft specification REV. D1.6, May 6th. 1993